2023
DESIGN AND VERIFICATION™
DVCON
CONFERENCE AND EXHIBITION
TAIWAN

NYCU, Hsinchu | September 7, 2023

DVCON TAIWAN 2023 CONFERENCE PROGRAM

Please visit website for more information!

https://dvcontaiwan.org

Sponsors and Organizers

accellera SYSTEMS INITIATIVE™

2023 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION TAIWAN

主辦單位
Organizer

accellera SYSTEMS INITIATIVE™

TICD Taiwan IC Design Society

協辦單位
Co-organizer

NYCU SoC 晶片系統研究中心

贊助單位
Sponsors

白金級 Platinum Sponsor

SYNOPSYS® cadence® SIEMENS

黃金級 Golden Sponsor

TESDA iSTART TalentPros 芯華章

Agenda

Time\Venue	International Conference Hall 國際會議廳	
09:00-09:20	**Opening** DVCon Taiwan 2023 Steering Committee	
09:20-09:50	**Keynote 1: Accellera, Standards, and Semiconductor Supply Chain** Lu Dai - Chair of Accellera and Senior Director at Qualcomm	
09:50-10:20	**Keynote 2: EDA 2.0 – Leveraging AI to Achieve the Next 10x** Dr. Paul Cunningham - Senior Vice President and General Manager, Cadence	
10:20-10:40	Morning Break	
10:40-11:10	**Keynote 3: Autonomous Verification: Are we there yet?** Ajay Singh - Senior Vice President, Synopsys	
11:10-11:40	**Keynote 4: Smart Verification: Faster is not enough!** Abhi Kolpekwar - VP & General Manager, Siemens EDA	
11:40-12:30	**Panel: How to Develop Future Talents in Design Verification** Language: Mandarin Moderator: Chen-Yi Lee, NYCU Panelists: Thomas Li, Synopsys; Simon Chang, Cadence; Philip Tsai, GUC; Chien Yeh, MediaTek	
12:30-13:30	Lunch Break	
Time\Venue	**International Conference Hall 國際會議廳**	**Conference Room 4 階梯教室**
13:30-14:00	**Paper 1.1 – Scalable Mixed Features Stimulus Generation for Cluster Network Using Sequence Decorator** Chi-Ming Li – Synopsys ARC DV	**Paper 2.1 – Tutorial – AI-Driven Verification** Tsung-Hsien (Curtis) Tsai - Cadence
14:00-14:30	**Paper 1.2 – UVM-based extended Low Power Library package with Low Power Multi-Core Architectures** Priyanka and Darshan - Silicon Interfaces	**Paper 2.2 – Tutorial – Debug Automation with AI** Craig Yang - Synopsys

Time\Venue	International Conference Hall 國際會議廳	Conference Room 4 階梯教室
14:30-15:00	**Paper 1.3 – Scoreboards and Checkers Memory, TLB and Cache** Rich Edelman - Siemens EDA	**Paper 2.3 – Reducing the simulation life cycle time of Fault Simulations using Artificial Intelligence and Machine Learning techniques on Big Data dataset** Gopi Srinivas Deepala - Silicon Interfaces
15:00-15:30	**Paper 1.4 – Improve the quality of SystemC IPs through coverage-driven random verification** Trung Pham – Renesas	**Paper 2.4 – Verification Challenges & Solutions of 10BaseT1s Automotive Ethernet PHY** Harshdeep Verma - Cadence
15:30-16:00	Afternoon Break	
16:00-16:30	**Paper 1.5 – SAR ADC Layout Generation Using Digital Place-and-Route Tools** Yao-Hung Tsai - NTU	**Paper 2.5 – Formal Sign-off methodology for IP blocks** Anna Chang - Google
16:30-17:00	**Paper 1.6 – Design and Verification of a Cell-Based PLL using an Optimized DCO** Yi-Sheng Wang - NTHU	**Paper 2.6 – A Novel Approach to Accelerate Latency of Assertion Simulations** Dr. Jack Yen - Synopsys
17:00-17:30	**Paper 1.7 – Building a Virtual Driver for Emulator** Chih Chiang Chen - Andes	**Paper 2.7 – Tutorial – Model Based Design** Dr. Alan P. Su - eNeural
17:30-18:00	Closing Session and Best Paper Award	
18:00-20:00	Dinner Party @Chinese restaurant at The Ho Hotel, 和選旅中餐廳	

More information in https://dvcontaiwan.org/program/

Keynotes

Lu Dai

Chair of Accellera and Senior Director at Qualcomm

Keynote 1

Accellera, Standards, and Semiconductor Supply Chain

Time: 9:20-9:50 | Room: International Conference Hall

Lu Dai is a Senior Director of Technical Standards at Qualcomm, leading Qualcomm's involvement in semiconductor standards and industry organizations. Lu was previously Senior Director of Engineering and led Qualcomm's SOC design verification team and front-end methodologies and initiatives. Lu was the Design Verification Lead responsible for multiple generations of Premium Tier lead chips at Qualcomm, including the best-selling Snapdragon 800 that powers Mars Perseverance rover and Ingenuity helicopter. He has been continuously working at Qualcomm for the past 15 years.

Prior to Qualcomm, Lu spent 11 years at Cisco serving as Design Verification Lead for its Gigabit Switching Business Unit where he worked on multiple generations of Cat4k ASICs. Lu started his career at Intel Architecture Lab.

Lu is also the current Chair of Accellera, an international standards organization in electronic design automation (EDA) and integrated circuit (IC) design and manufacturing. He is the longest serving Chair of Accellera since 2017 and served on its Board of Director since 2015.

Lu holds a Master's degree in Electrical Engineering from Cornell, and a Bachelor's in Electrical Engineering and Computer Science from UC Berkeley.

Abstract: A review of Accellera's history and standards. A discussion on semiconductor supply chain challenges. And an outlook for the future and how standards development relates to supply chain sustainability.

Paul Cunningham

Senior Vice President and General Manager, Cadence

Keynote 2

EDA 2.0 – Leveraging AI to Achieve The Next 10x

Time: 9:50-10:20 | Room: International Conference Hall

Dr. Paul Cunningham has served as Senior Vice President and General Manager of the System Verification Group (SVG) in Cadence since March 2021, running the division since 2018. His responsibilities include logic simulation, emulation, prototyping, formal verification, Verification IP, and functional debug. Prior to this role, Cunningham was responsible for Cadence's frontend digital design tools including logic synthesis and design-for-test.

Dr. Cunningham joined Cadence in 2011 via the acquisition of Azuro, a startup developing concurrent physical optimization and useful skew clock tree synthesis technologies, where he was a co-founder and CEO. Dr. Cunningham holds a MS and a PhD in Computer Science from the University of Cambridge in the UK.

Abstract: IC device complexity continues to increase, driven by expanding demand for SoCs across industries like hyperscale compute, automotive, IoT, aerospace, and mobile. Increased complexity and demand for devices has resulted in more design starts, with not enough engineering resources to meet the demand. As Artificial Intelligence and Machine Learning become more and more accessible across the technology landscape, EDA has the opportunity to leverage these technologies to increase overall productivity through both automation, and catalyzation of the human in the loop. Cadence SVP and GM Paul Cunningham will discuss this current IC landscape, and how AI can help EDA drive the next 10x increase in engineering productivity.

Ajay Singh

Senior Vice President, Synopsys

Keynote 3

Autonomous Verification: Are we there yet?

Time: 10:40-11:10 | Room: International Conference Hall

Ajay Singh is senior vice president and leader of the Design Creation and Verification (DCV) Group at Synopsys. Ajay leads the Synopsys R&D team responsible for developing EDA tools for design synthesis (Design Compiler, Fusion Compiler), design exploration (RTL Architect), logic equivalence (Formality), dynamic simulation (VCS), static verification (VC SpyGlass), formal verification (VC Formal), debug (Verdi), and fault simulation (VC Z01X).

Ajay holds a bachelor's degree in Electronics and Telecommunication from College of Engineering, Pune, India. He has 30+ years of EDA industry experience.

Abstract: We are now in the world of Smart Everything from voice assistants, advanced robotics, drone-based delivery to autonomous cars and chatbots. This begs the question, how are we doing in design verification? Design verification is one of the most expensive and time-consuming activities for any chip design. Moreover, every year the cost of design verification grows exponentially and despite that ½ of design re-spins are caused by functional or logic bugs. When we consider where time is spent in verification, coverage convergence and debug consume 70% of overall verification time. In addition to time spent, misinterpretation of specifications is a major source of bugs. With the rapid evolution of AI/ML technologies, how can we automate some or many of these activities? What technologies are available today and what is on the horizon? With the advent of Large Language Models (LLM) and Generative Pre-Trained Transformer (GPT) models, what are the possibilities in design verification? Just like there are 6 levels of driving automation, from driver assistance to conditional automation to full automation, what level is the current state of verification? This keynote address will explore these topics and look ahead to the future of autonomous verification.

Abhi Kolpekwar

VP & General Manager of Digital Verification Technologies, Siemens EDA

Keynote 4

Smart Verification: Faster is not enough!

Time: 11:10-11:40 | Room: International Conference Hall

Abhi Kolpekwar is a Vice-President and General Manager responsible for Digital Verification Technologies (DVT) division at Siemens EDA (Formerly Mentor Graphics). Abhi's organization covers Simulation, Formal, Functional-Safety, Portable-Stimulus, Coverage Acceleration, Static Verification, Design Creation, Debug, and Verification IP product lines with teams across the globe. These technologies serve world's premium electronic design companies in Aero-Space Defense, Automotive, Wireless, Storage, Processors, IoT and AI markets and many more.

Abhi graduated from Carnegie Mellon University with MS in Electrical & Computer Engineering. Abhi also holds MS in Physics and has authored 13 US patents in functional verification area. Abhi has over 25 years of experience with development and management of very large-scale software solutions and leading global organizations. Abhi has a track record of innovation by taking ideas from concept to realization in an agile development environment. Abhi is passionate about building strong and highly collaborative work environment and helping engineers develop into highly productive professionals and effective leaders. Abhi joined Mentor Graphics in 2015 where he was responsible for engineering, operations and quality before stepping into the GM role. Abhi's 25 plus year career in EDA covers a wide range of roles including technology development, corporate strategy, solutions development and pre-sales in functional verification area.

Abstract: Buckle up, fellow tech explorers! The ever-changing landscape of semiconductor design is calling for a cosmic paradigm shift in how we conquer upcoming verification challenges. Sure, we've zoomed towards faster and more efficient verification methodologies thanks to tech wizardry, but we can't warp past the fact that sheer speed alone won't guarantee us complete solutions. As we reach for new frontiers, the complexity of design and verification tasks skyrockets, beaming us towards an urgent need to harness the power of intelligence. Get ready for a keynote that takes you on a thrilling journey, exploring the vital role of smarter solutions in the design and verification process. It's not just about speed, fellow adventurers! We'll boldly discuss the factors that highlight the limitations of solely relying on speed, all while shining a spotlight on the pressing demand for intelligent EDA solutions. Brace yourselves for a universe of possibilities, where performance optimization and tackling intricate design and verification challenges go hand in hand with intelligent solutions.

Panel

How to Develop Future Talents in Design Verification
高峰論壇: 如何培養未來設計驗證人才

Moderator	*Chen-Yi Lee*	李鎮宜副校長 - NYCU 陽明交通大學
Panelists	*Thomas Li*	李新基副總 - Synopsys 台灣新思科技
	Simon Chang	張永專資深協理 - Cadence 益華電腦
	Philip Tsai	蔡明甫處長 - GUC 創意電子
	Chien Yeh	葉建勳處長 - MediaTek 聯發科技

Abstract:

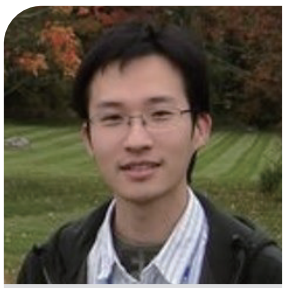
5G、無所不在的AI以及高性能運算等新興應用，帶來了對複雜晶片與電子系統設計的需求，也使得設計驗證工作變得更具挑戰性。在此同時，產品上市時程的壓力與來自客戶的要求不減反增，這意味著驗證工程師必須要在非常有限的時間內完成比以往更艱鉅的任務。 究竟當前的設計驗證工作需要具備哪些能力與特質的人才？企業組織該如何培養、訓練無論是現有團隊或新進人員，以因應驗證任務需求，又有哪些技術資源與工具可以利用？在這場高峰論壇中，來自產業界領導業者與學界的與談人，將從分享他們對於今日設計驗證任務所面臨的艱鉅挑戰之觀察出發，並針對產業界能如何攜手合作紓解工程人才短缺、以及透過更具效益的方式完成驗證任務等議題進行深入的探討。

2023 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION TAIWAN

Conference Information

Steering Committee

Penny Yang
Synopsys
General Chair



Ying-Cherng Lan
Cadence
Vice Chair

Michael Chiang
Siemens
Exhibit Chair

Jimmy Liu
NYCU EE
Technical Program Chair

Alan Su
eNeural
Marketing Chair

Robert Chen
TESDA
Marketing Co-Chair

Yung Jen Chen
Realtek
Program Chair

SJ Wu
Andes
Program Co-Chair

Leo Chen
Nvidia
Keynote Chair

Prosper Chen
AMD
Tutorial Chiar

Jim Kung
MediaTek
Panel Chair

WiFi at DVCon Taiwan

Network Name: **NYCU-Guest**
Register and get password by message.

Networking Receptions

*Required DVCon Taiwan badge

Welcome Reception
Level 1, in front of Registration
8:30 am-9:00 am

Morning Break
Level 1, in front of Registration
10:20 am-10:40 am

Lunch Break
Level 1, in front of Registration
12:30 pm-1:30 pm

Afternoon Break
Level 1, in front of Registration
3:30 pm-4:00 pm

Dinner Party
Chinese restaurant at The Ho Hotel, 和選旅中餐廳
https://www.thehohotel.com.tw/
新竹市東區大學路16號2F
6:30 pm-8:00 pm

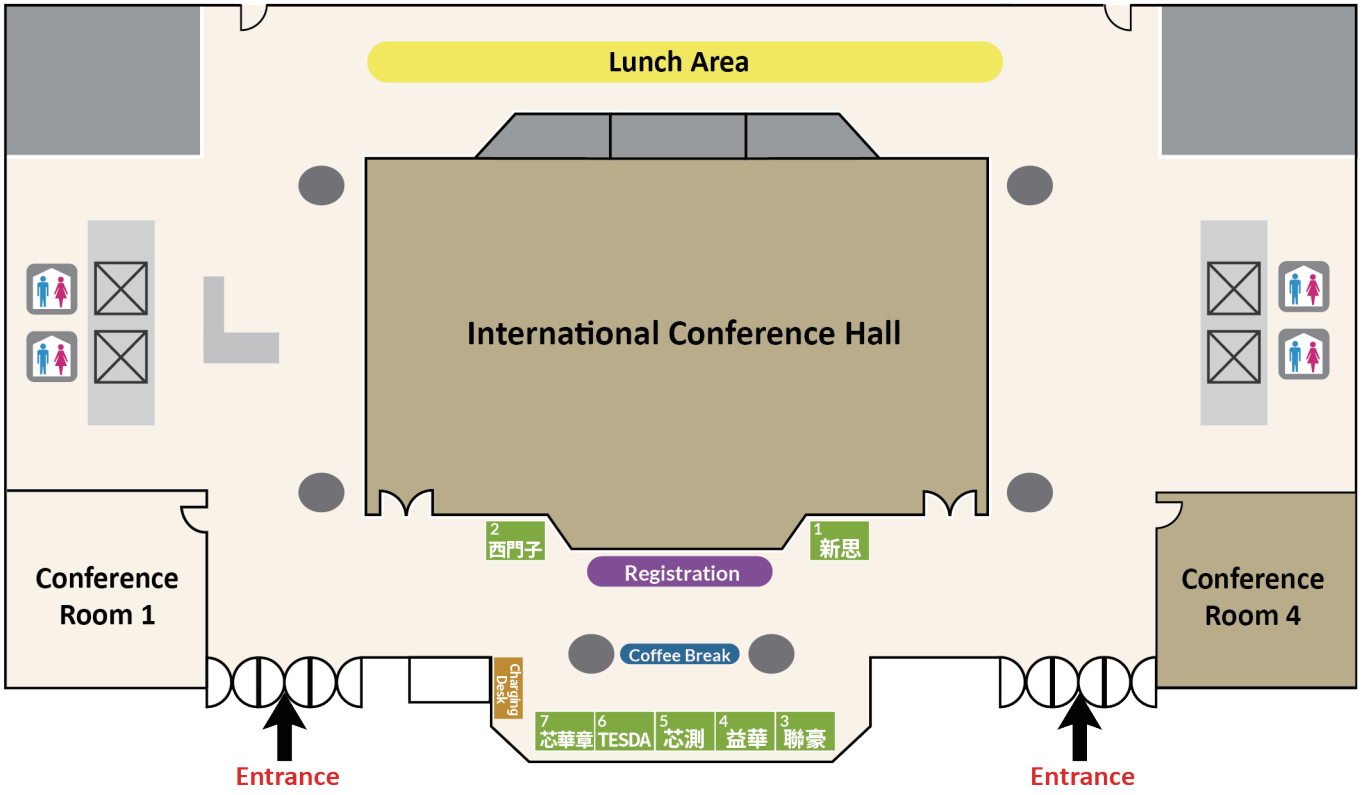
Closing session and Best Paper Award

Best Paper and Outstanding Awards
Recycle your badge and lanyard before you leave

2023 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION TAIWAN

Exhibit Hours

Exhibit Halls on Level 1
Exhibits Open: 10:00 am – 4:00 pm



1 SYNOPSYS®
2 SIEMENS
3 TalentPros
4 cadence®
5 iSTART
6 TESDA
7 芯華章
充電桌 Charging Desk

Notes

2023 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION TAIWAN

Notes

SYNOPSYS®

Synopsys VSO.ai

- Automate discovery of elusive gaps in test coverage
- Explore infinite design states
- Focus on fixing bugs, not finding them

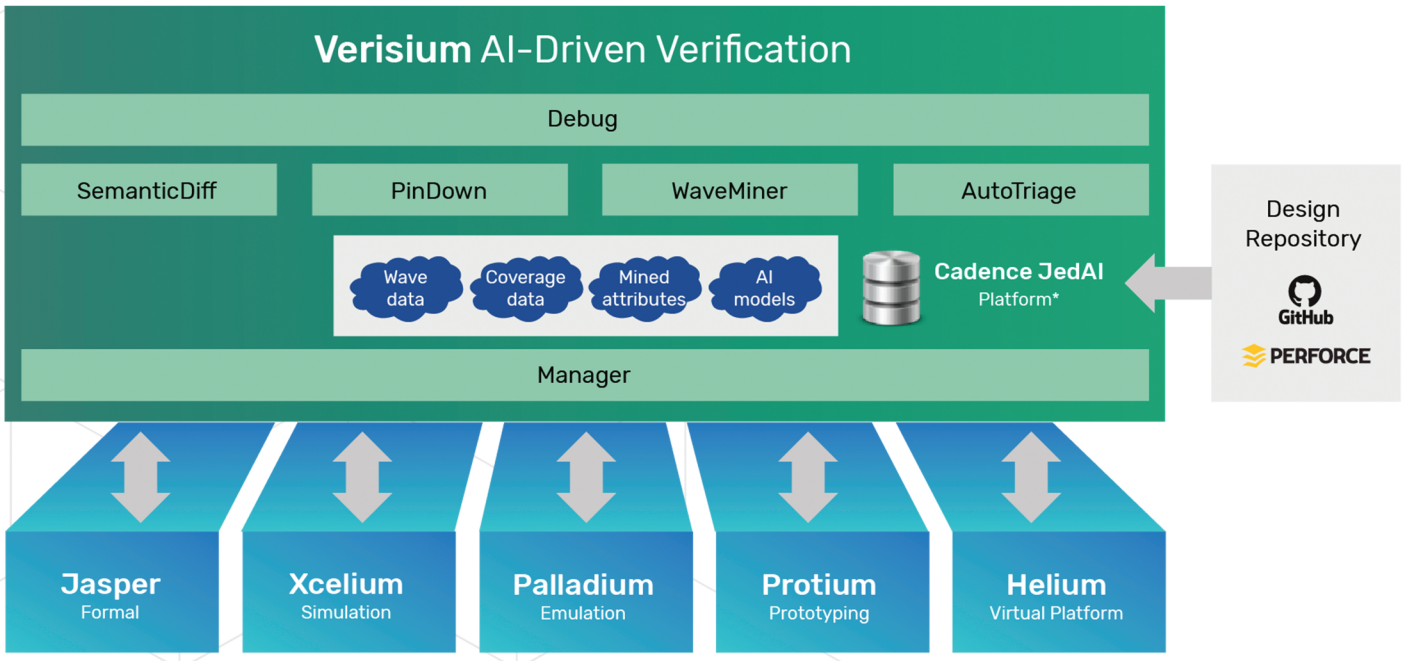
Learn More

cadence®

Cadence Revolutionize Verification

Verisium AI-Driven Verification Platform

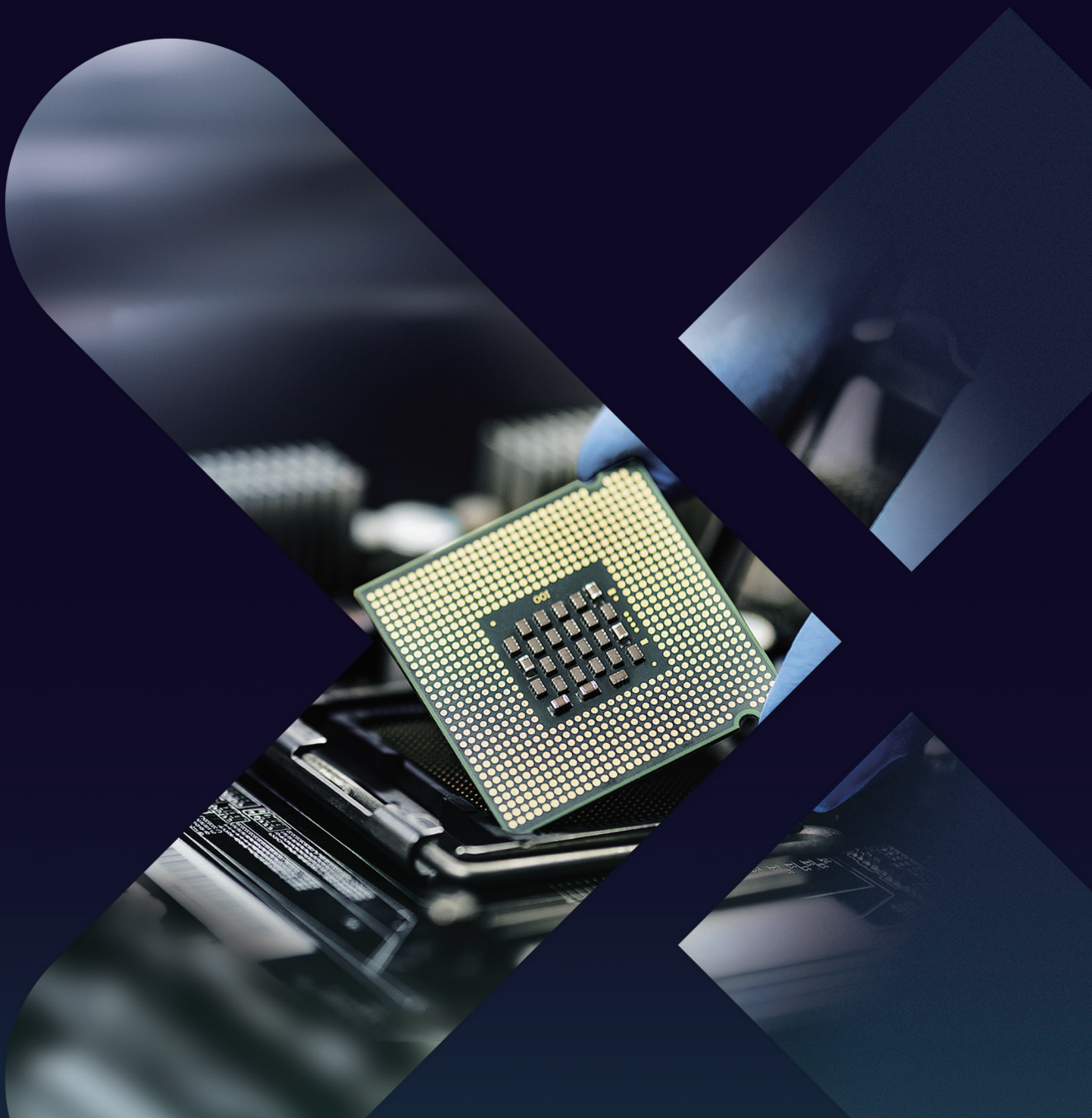
LEARN MORE



*Cadence Joint Enterprise Data and AI (JedAI) Platform

SIEMENS

Engineer a smarter future faster with Siemens EDA



TESDA

台灣電子系統設計自動化股份有限公司

Who is TESDA?

TESDA 是一家創新驅動的科技公司，致力於 RTL SoC 驗證自動化設計工具開發並提供高品質驗證流程及服務。

TESDA is an innovation-driven technology company dedicated to the development of RTL SoC verification automation tool and providing professional verification and flow establishment services.

Mission

Boost SoC DV efficiency with easy-to-use verification tool and open ecosystem.

Product

AutoDV: Automatic RTL testbench generator for SoC and subsystems.

Service

Professional RTL verification service, from SoC, subsystem to IP level verification.

https://www.tes-da.com/

03-5910000 | service@tes-da.com | 統一編號 83045088

新竹縣竹東鎮中興路四段195號 工業技術研究院 53 館 402 室

iSTART
芯測科技股份有限公司

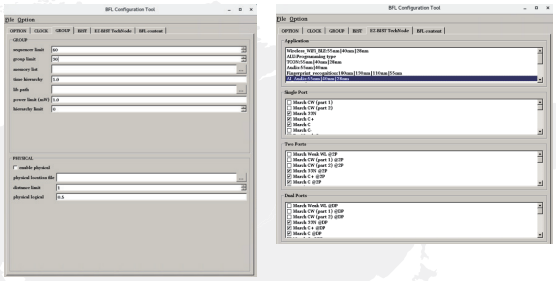
客製化EDA工具&客製化IP

START™ v3

START™ v3提供豐富的記憶體測試功能與記憶體修復解決方案。包含Hard-Repair (硬式修復)與Soft-Repair (軟式修復)兩種高效率的記憶體修復技術，透過Hard-Repair和Soft-Repair可大幅提升SoC (系統晶片)的良率與競爭力。

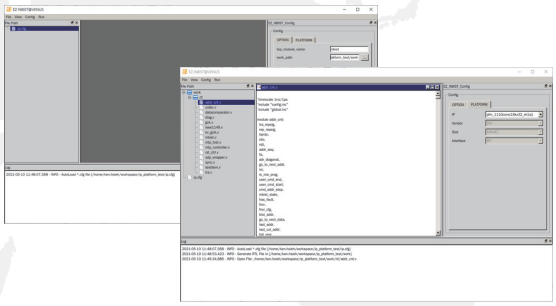
EZ-BIST

內建豐富的記憶體測試算法，透過GUI (圖形化使用者介面)即可完成記憶體電路設計的客製化EDA工具，能根據晶片的製程與應用，選擇最適當的算法。



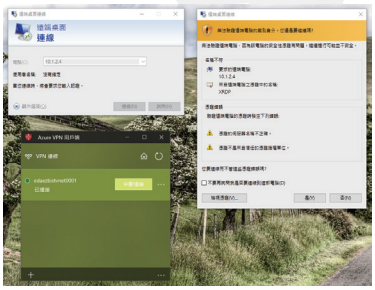
EZ-NBIST

透過GUI (圖形化使用者介面)即可完成NVM (非揮發性記憶體)電路開發的客製化EDA工具，能大幅縮短NVM IP的測試與修復時間、降低晶片測試成本。



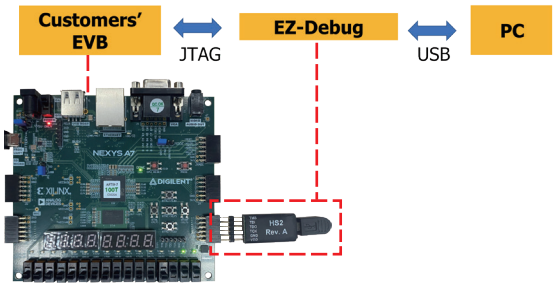
EDA tools clouding service

採用訂閱制即可連結EDA工具的服務平台，透過安全防禦系統的保護，讓使用者可以安心使用雲端EDA工具，並完成記憶體測試電路的開發。



EZ-Debug

EZ-Debug是高性價比的晶片記憶體診斷工具，針對開發中與非量產的晶片，進行晶片內的記憶體測試，能立即得知診斷結果。



www.istart-tek.com
Business:sales@istart-tek.com
Technical:support@istart-tek.com

Website

TalentPros

YOUR TRUSTED PARTNER FOR FPGA SOLUTION EXPERTISE

Bringing Efficiency and Precision to Circuit Design

About Us

Founded in 2017, TalentPros System Innovation Co., Ltd (TPSIC) is a leading Taiwan-based FPGA prototyping services provider, and with the mission of designing and manufacturing professional system circuitry and application design in FPGA products.

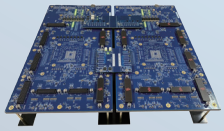
AMD Xilinx FPGA based Prototyping Solutions

- ✓ VU19P FPGA Prototyping Platform
- ✓ VU29P FPGA Prototyping Platform
- ✓ VU9P FPGA Prototyping Platform
- ✓ KU085 FPGA Prototyping Platform
- ✓ KU040 FPGA Prototyping Platform
- ✓ Zynq UltraScale+ RFSoC Platform
- ✓ Zynq-7 Module

UNLEASH INNOVATION WITH TALENTPROS

01 FPGA Prototyping Solutions

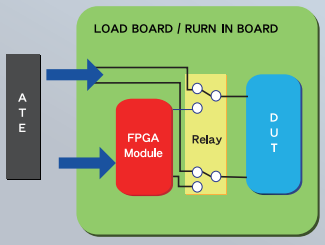
Taiwan's Premier FPGA Prototyping Platform
Xilinx Virtex UltraScale+ / Kintex UltraScale / Zynq-7


VU19P Expansion


VU19P


VU9P/VU29P

02 BOST Module Solutions



Reducing Testing Costs
Expanding Automatic Test Equipment (ATE) Functionality and Channels

03 Customized FPGA Board Design Service

- Embedded Circuit design, SOC, ADC, DAC, high speed transceiver
- PCB Layout design (material, stackup)
- PCB Assembly &Final Test

FPGA Module


TXZ-1120


TXZ-1320


TXZ-1300

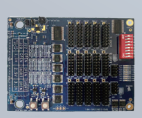

BOST Module

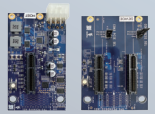

KU040 Module

Daughter Board


USB 3.0 PHY Board


Customized MIPI PHY Board

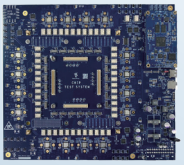

IO Board

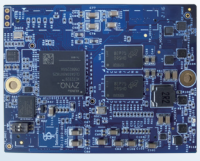

PCIe Board


HDMI 2.1


DP 1.4

FPGA-Based Customized Service


Desktop ATE

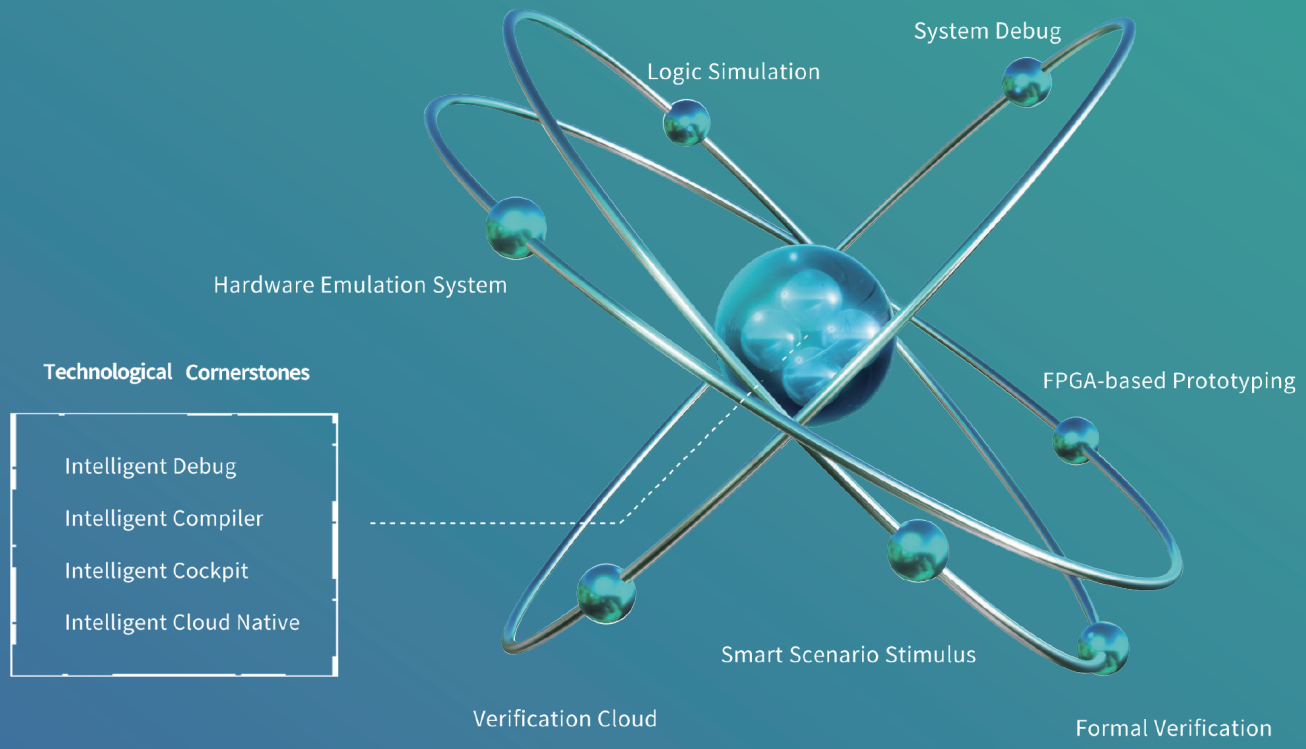

FPGA Module

Contact Us : +886 35586851
4F., No. 550, Xianzheng 2nd Rd., Zhubei City, Hsinchu County 302, Taiwan (R.O.C.)

X-EPIC

Accelerating System Verification

Together with our partners, we are pursuing to bring the EDA industry to an entirely new level by injecting the power of Artificial Intelligence, Machine Learning, Cloud Native, and other leading-edge technologies, which can enormously simplify and lower down the bar of the current IC design. In the end, it shortens the development cycle or time-to-market of the product.



Contact Us

Follow X-EPIC for the Latest News.

X-EPIC Website: www.x-epic.com

E-mail

Sales: sales@x-epic.com

Overseas: global@x-epic.com

Marketing: communications@x-epic.com

Human Resources: career@x-epic.com

Follow X-EPIC on Wechat

X-EPIC Official Website

accellera SYSTEMS INITIATIVE™

TICD Taiwan IC Design Society

協辦單位 Co-organizer

NYCU SOC 晶片系統研究中心

贊助單位 Sponsors

SYNOPSYS® cadence® SIEMENS TESDA iSTART TalentPros 芯華章