

FIRST DVCON IN TAIWAN!

WELCOME TO DVCON TAIWAN

2023-09-07 – NYCU, HSINCHU

新竹陽明交通大學電資大樓

The Design & Verification Conference & Exhibition is the premier conference on the application of languages, tools, methodologies and standards for the design and verification of electronic systems and integrated circuits.

Congratulations & Thank You to the Organizers & Participants



SYNOPSYS®

Autonomous Verification: Are We There Yet?

Ajay Singh

SVP of Engineering, Design Creation & Verification

Question for ChatGPT

What is Autonomous Verification?

“Autonomous Verification refers to the process of automatically verifying and validating systems, software or components *without significant human intervention*. It involves utilizing automated tools, algorithms, or systems to assess the correctness, performance, safety, or compliance of a particular entity or process...”

Robotaxi expansion gets green light in San Francisco

11 August

BBC NEWS



Autonomous Taxis Are Here Today

LEVELS OF DRIVING AUTOMATION



0	1	2	3	4	5
No Automation	Driver Assistance	Partial Automation	Conditional Automation	High Automation	Full Automation
The Human performs all the driving tasks	The Vehicle features a single automated task (e.g cruise control)	The Vehicle features multiple automated tasks, but Human involvement is needed for other tasks	The Vehicle can perform most driving tasks, but Human override is still required	The Vehicle performs all driving tasks under specific circumstances. Human override is an option	The Vehicle performs all driving tasks without any Human intervention or attention

The Human monitors the driving environment

The Vehicle monitors the driving environment

LEVELS OF VERIFICATION AUTOMATION

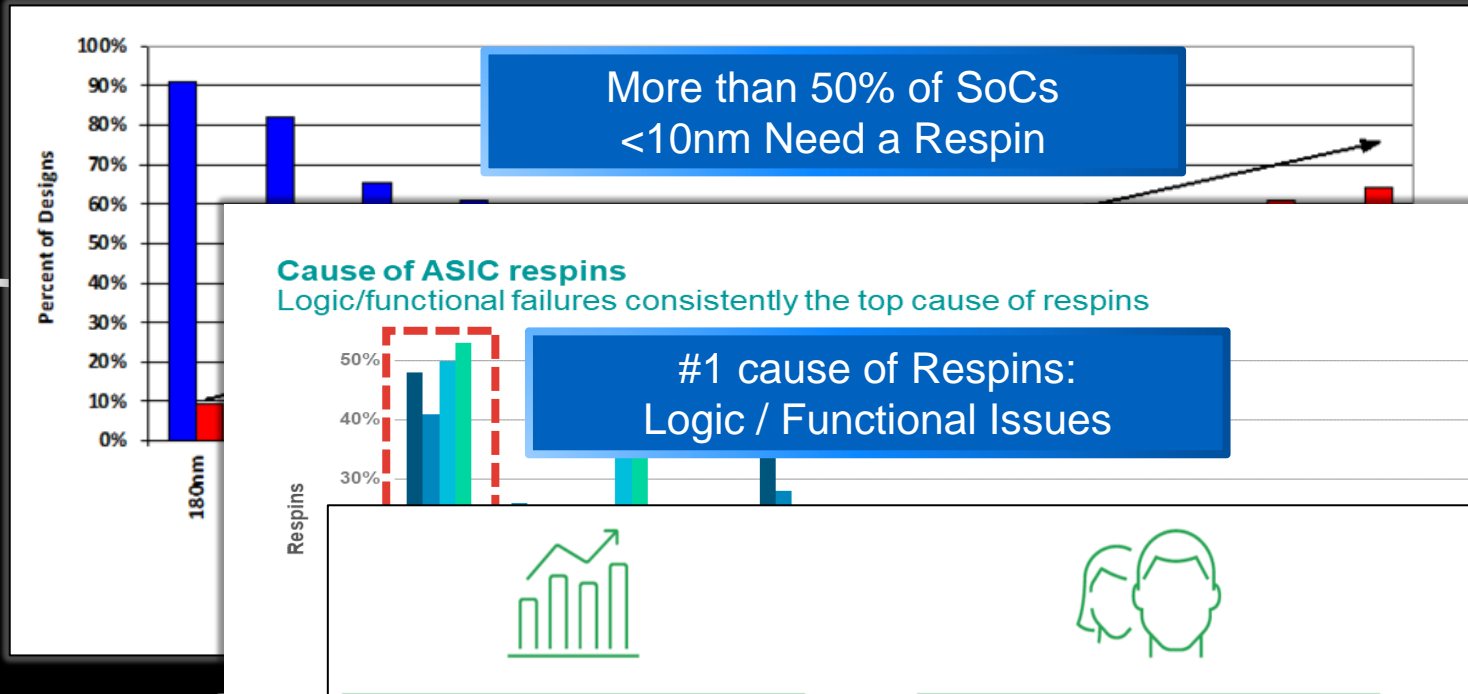


0	1	2	3	4	5
No Automation	Engineer Assistance	Partial Automation	Conditional Automation	High Automation	Full Automation
The Human performs all the Verification tasks	The tool features a single automated task (e.g Constraint Random Verification)	The tool features multiple automated tasks, but Human involvement is needed for other tasks	The tool can perform most verification tasks, but Human overview is still required	The tool performs all verification tasks for certain kind of designs. Human override is an option	The tool performs all verification tasks without any Human intervention or attention

The Human controls the scope of Verification

The Tool controls the scope of Verification

Do We Need Autonomous Verification?



Schedule & TTM

Design & Verification Engineers / Project

Source: BCG analysis

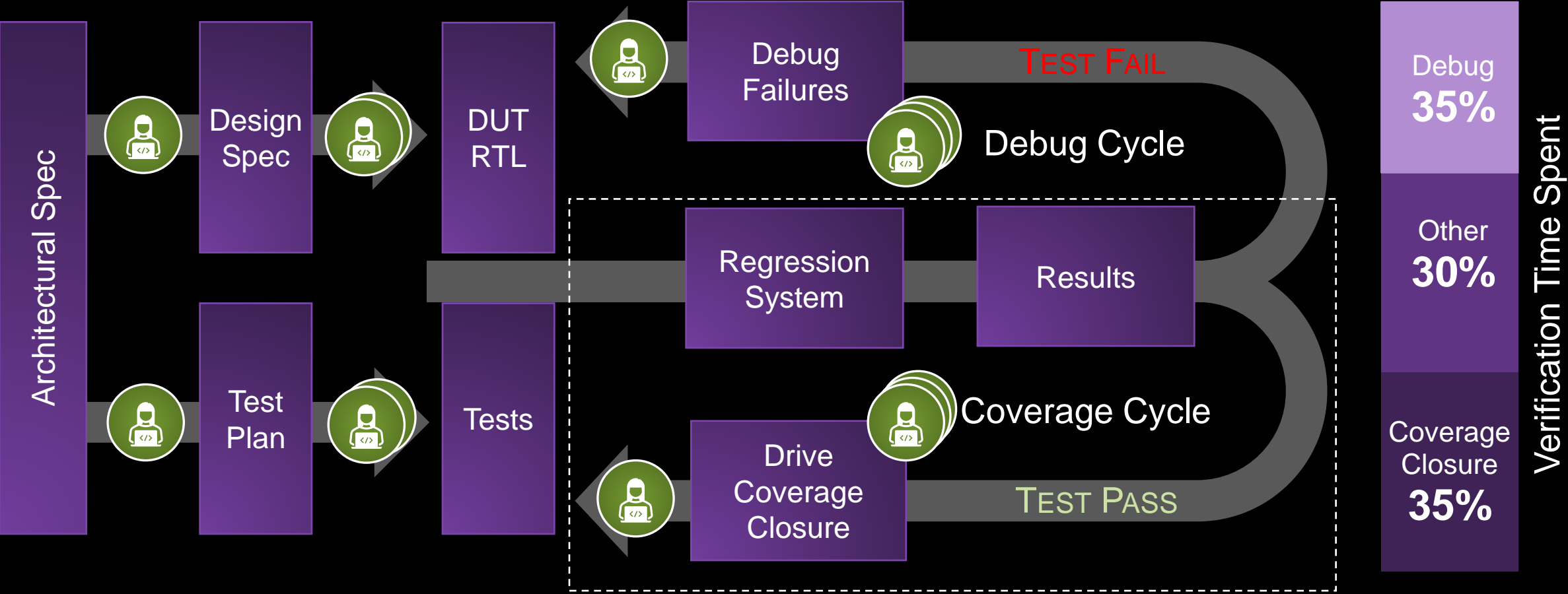
89,000	66,000	23,000
Demand for workers is expected to rise by ~50% While supply will grow by less than 1% annually Meaning that demand for design workers will exceed supply by nearly 35% in 2030

Yes! Autonomous Verification is Needed to Address Complexity

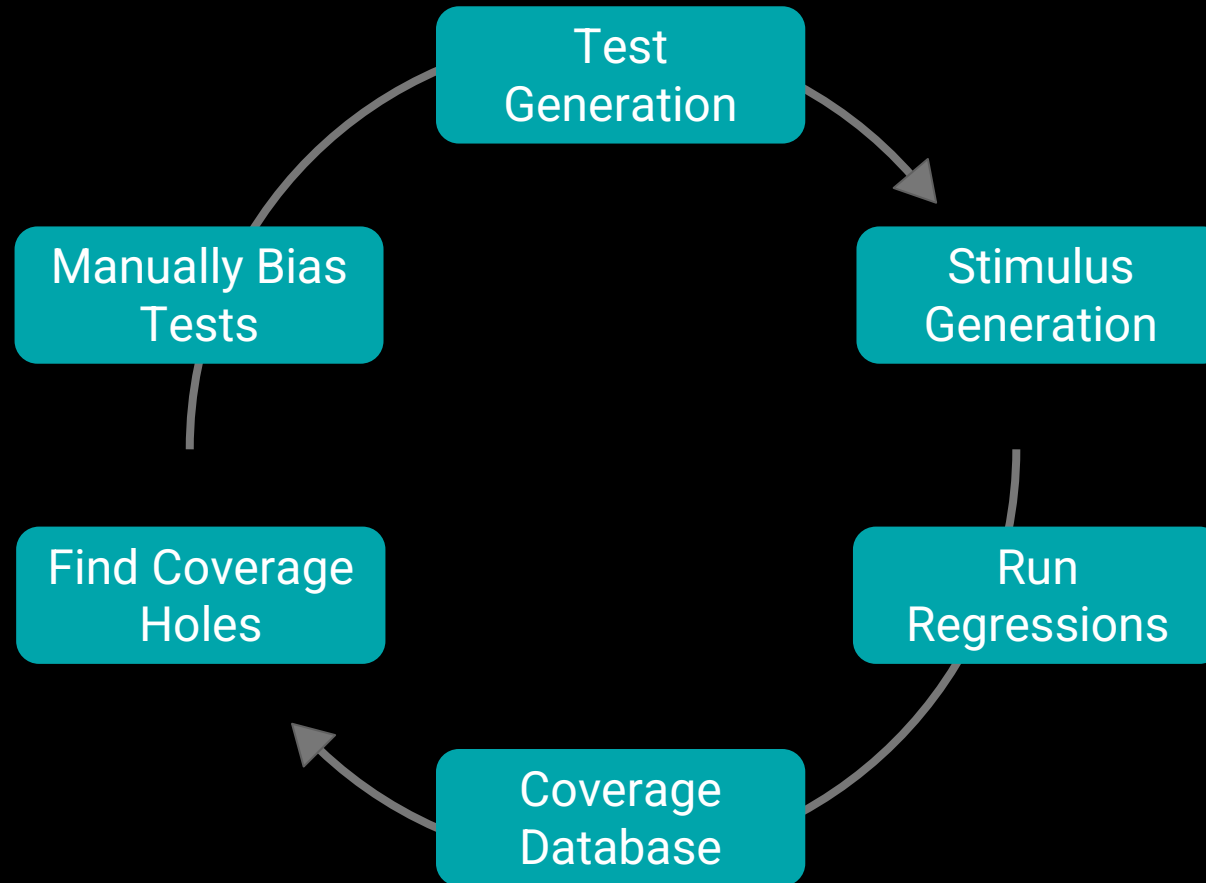
Design size & Verification Complexity Explosion

Time

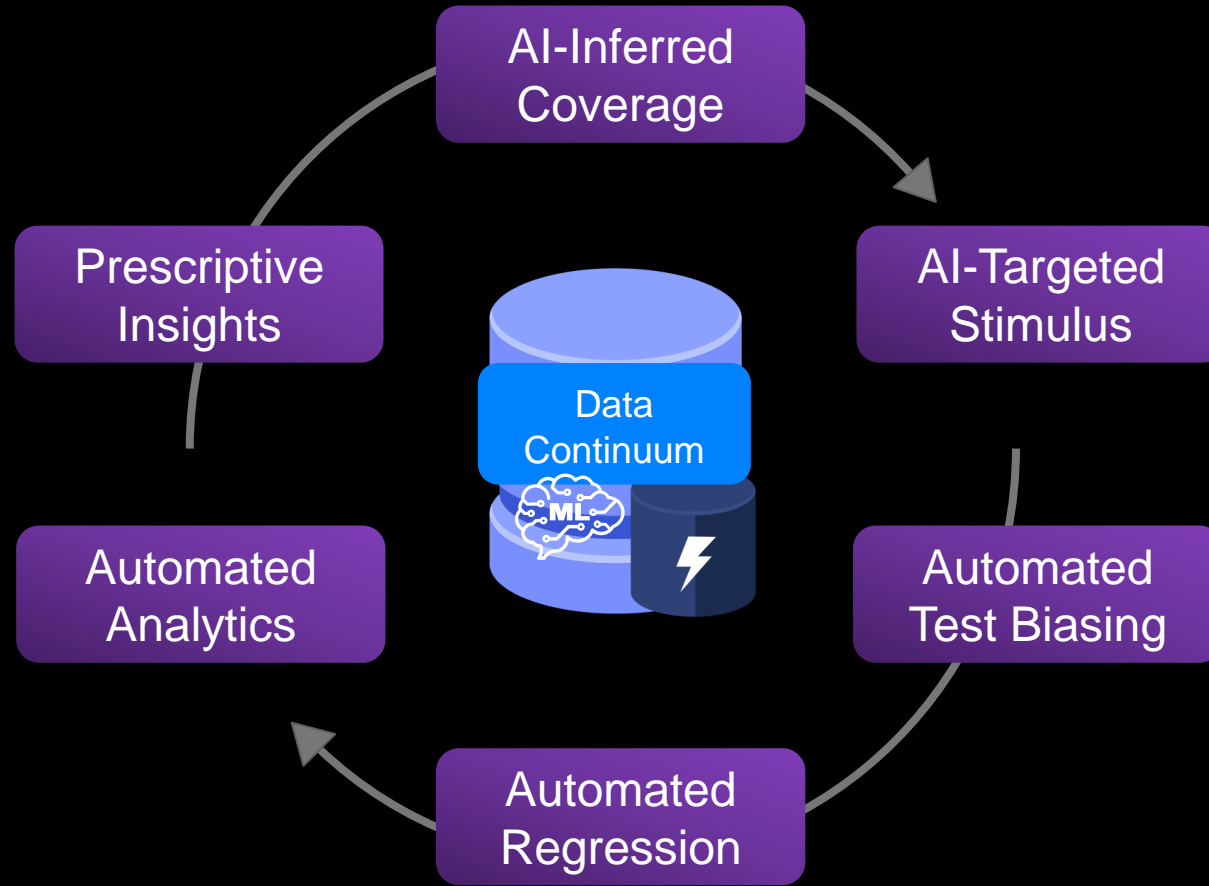
Where can we do automation in Verification?



Typical Coverage Flow

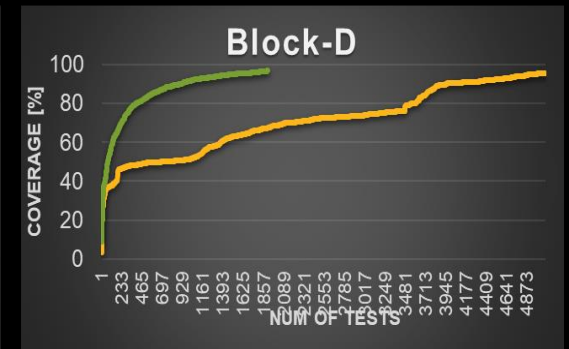
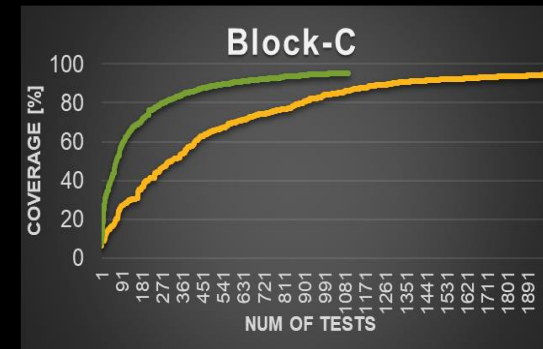
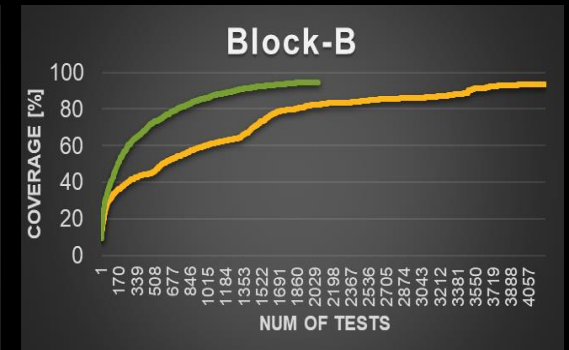
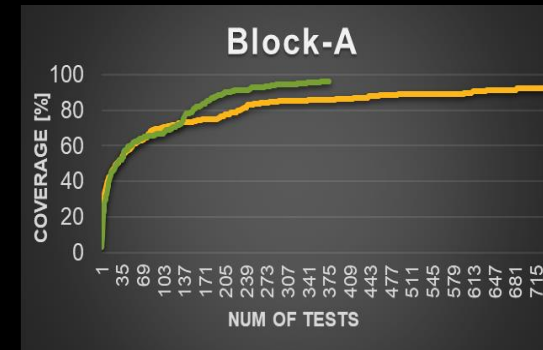
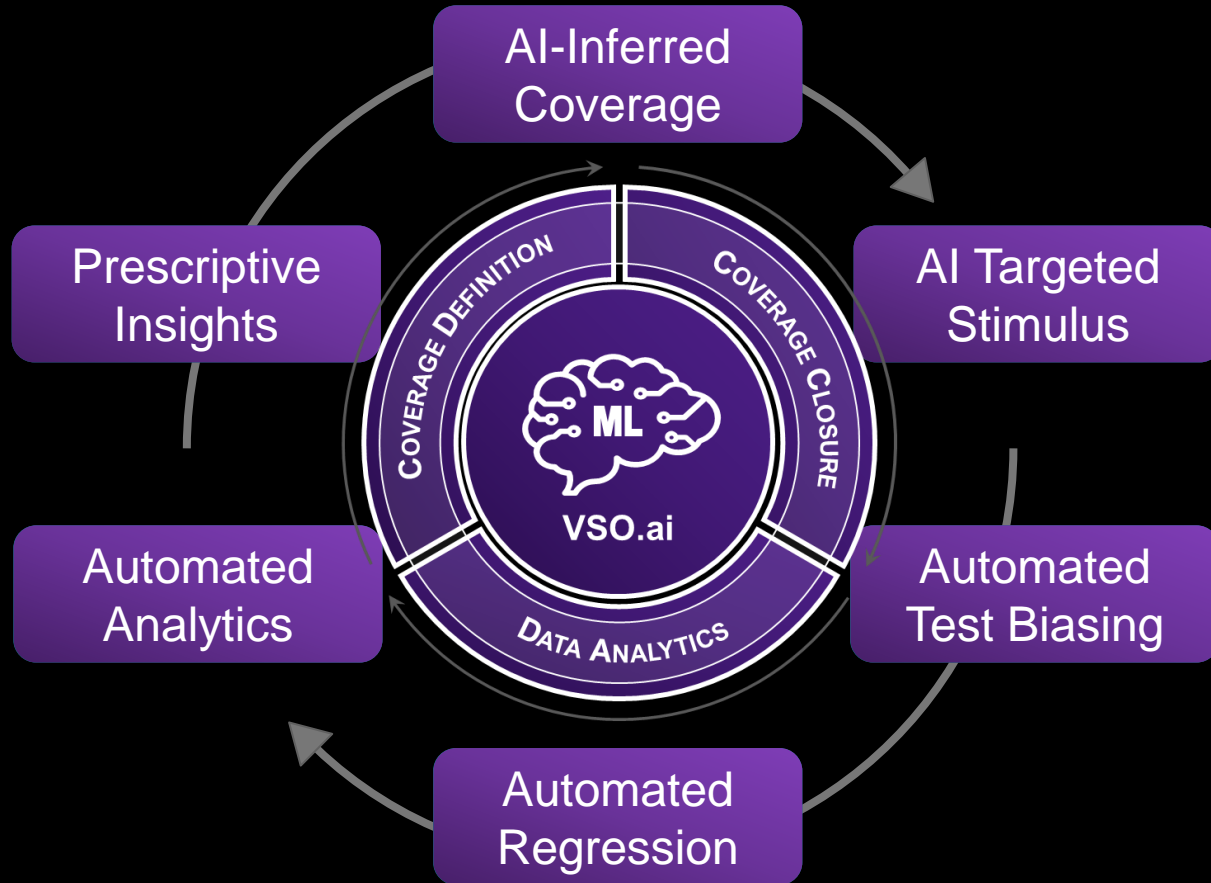


AI Assisted Coverage Flow



VSO.ai: Autonomous Coverage Closure

Accelerating coverage closure upto 3x-5x



With VSO.ai ———

Without VSO.ai ———

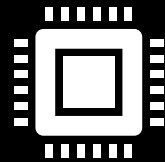
VSO.ai: Customer Results

Faster Closure and Higher Coverage

10-15%
Higher
Coverage



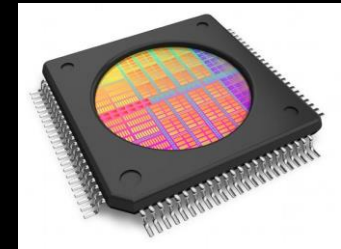
Automotive



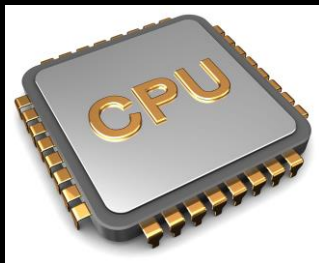
IP Provider

26%
Higher
Coverage

3X
Reduction
In Tests



Memory



Processor

2X
Reduction
in Tests

68%
Reduction
in Tests



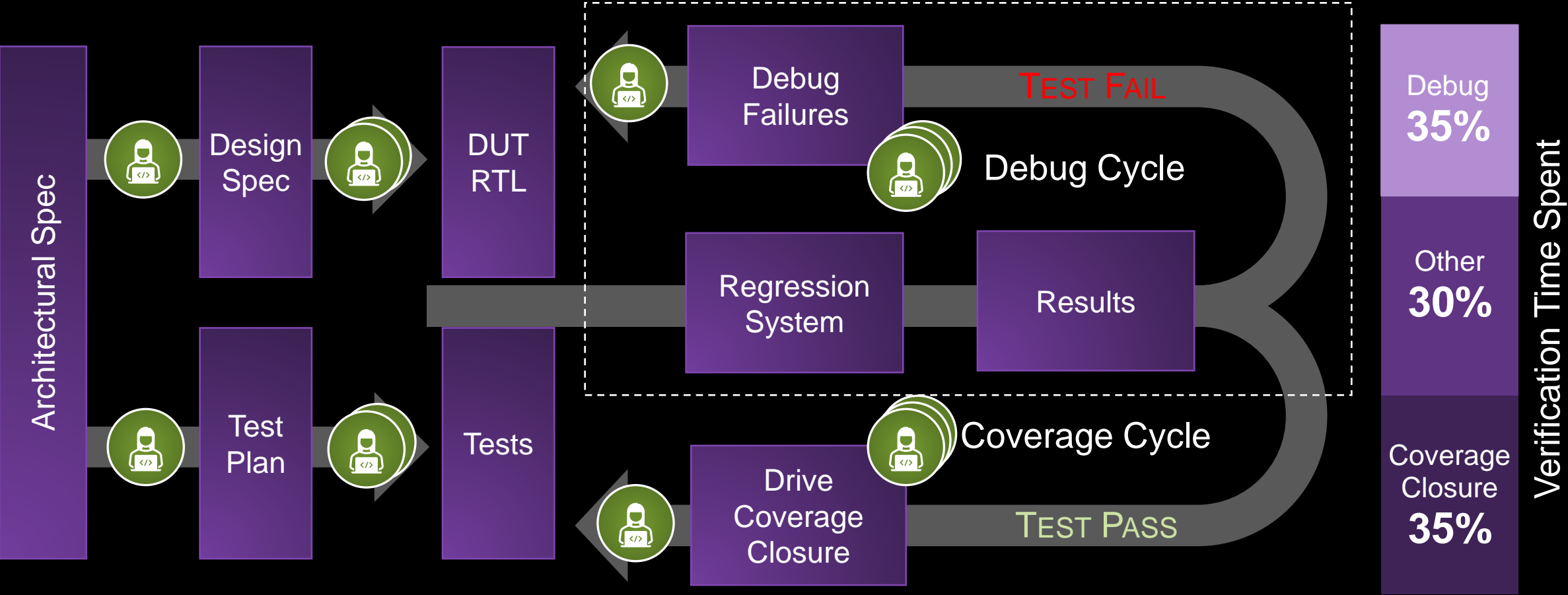
Mobile SoC

5-10X
Reduction
In Tests

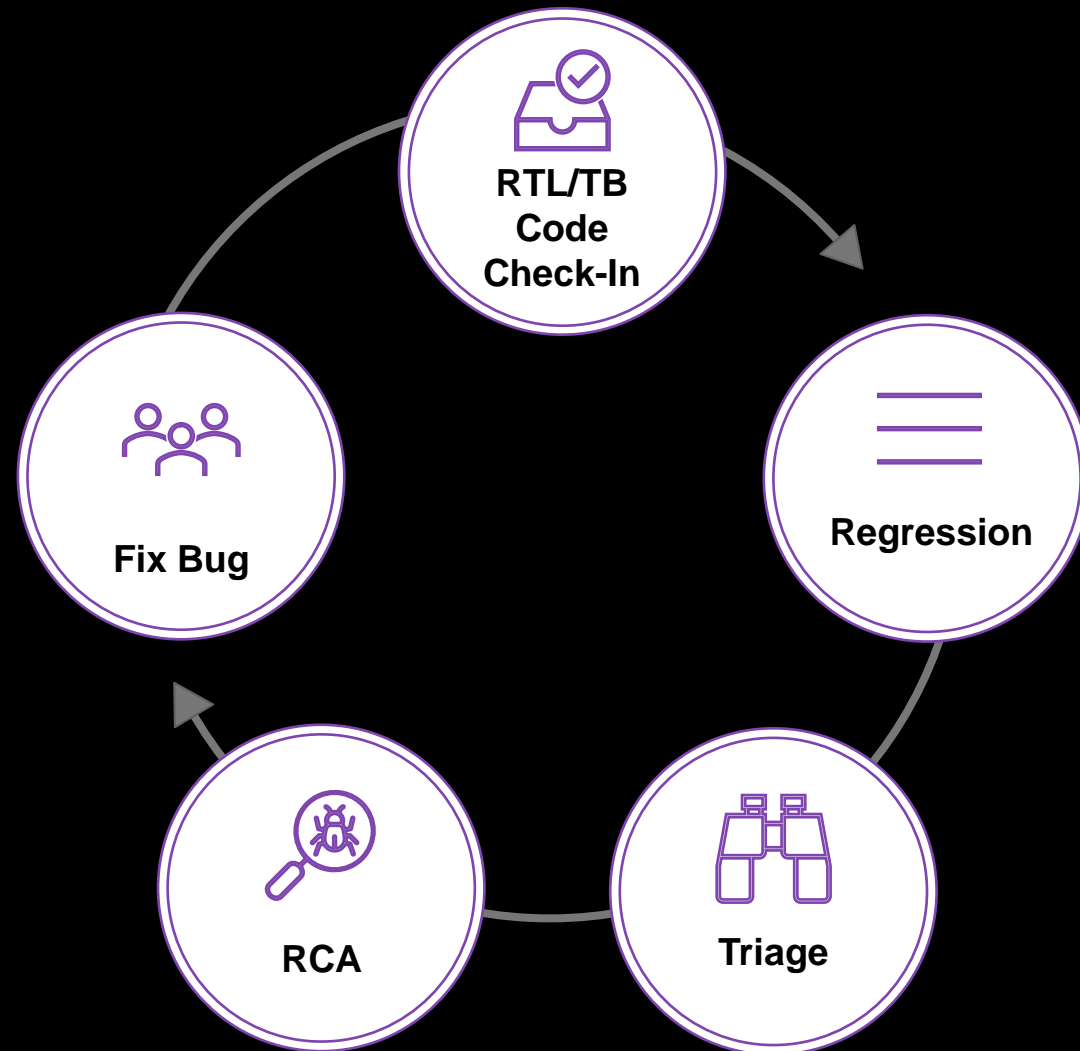


AP Mobile

How is Debug Automated Today?

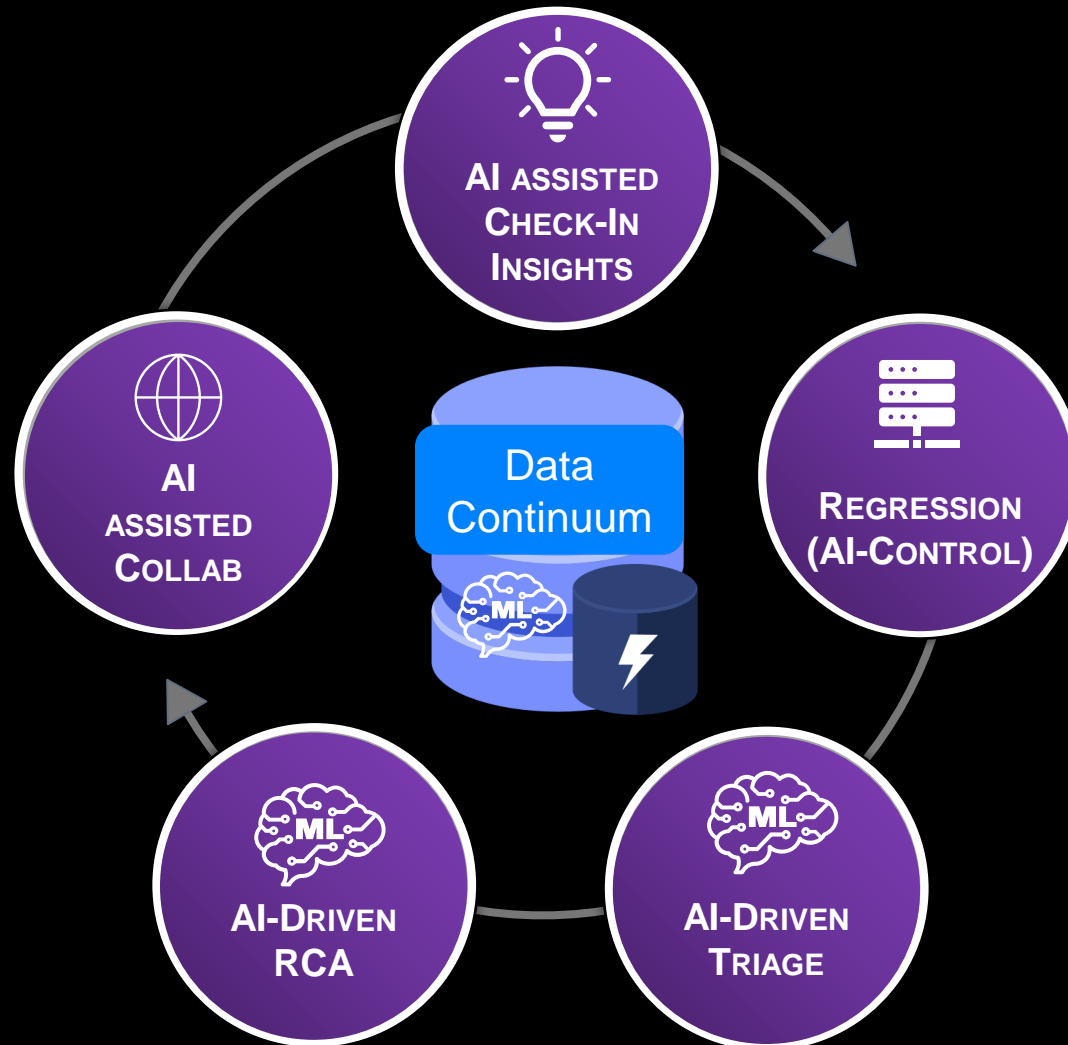
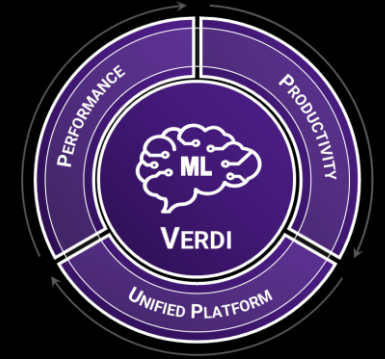


Typical Debug Flow



AI Assisted Debug Flow

Next-Generation Verdi: Improves debug productivity up to 10X



Next-Gen Verdi: Accelerate Debug Automation

Customer Examples



Automotive

Gate-level
with Many Xs

60x

XRCA Engine



Video

DUT
Code Change

20x

DUTRCA Engine



Server

Multiple Failing
Assertions

10x

DUTRCA Engine

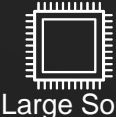


Graphics

DFT with
X Monitors

10x

XRCA Engine



Large SoC

Massive
Log Files

5x

ML-Binning



Video

DUT Hang

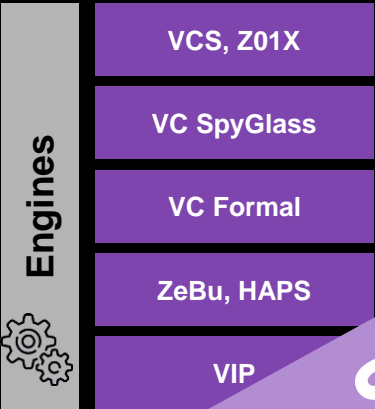
48x

DUTRCA Engine

Introducing Next-Generation Verdi Platform



See the demo in the Synopsys booth!



Innovative Debug

- AI-Based RCA
- Intelligent Debug Collaboration

Design Verification

- Smart Code Template
- Testbench Lint
- Design Lint

Verification Management

- Enterprise Planning
- Coverage Aggregator
- Test Optimization
- Manager and Dashboard

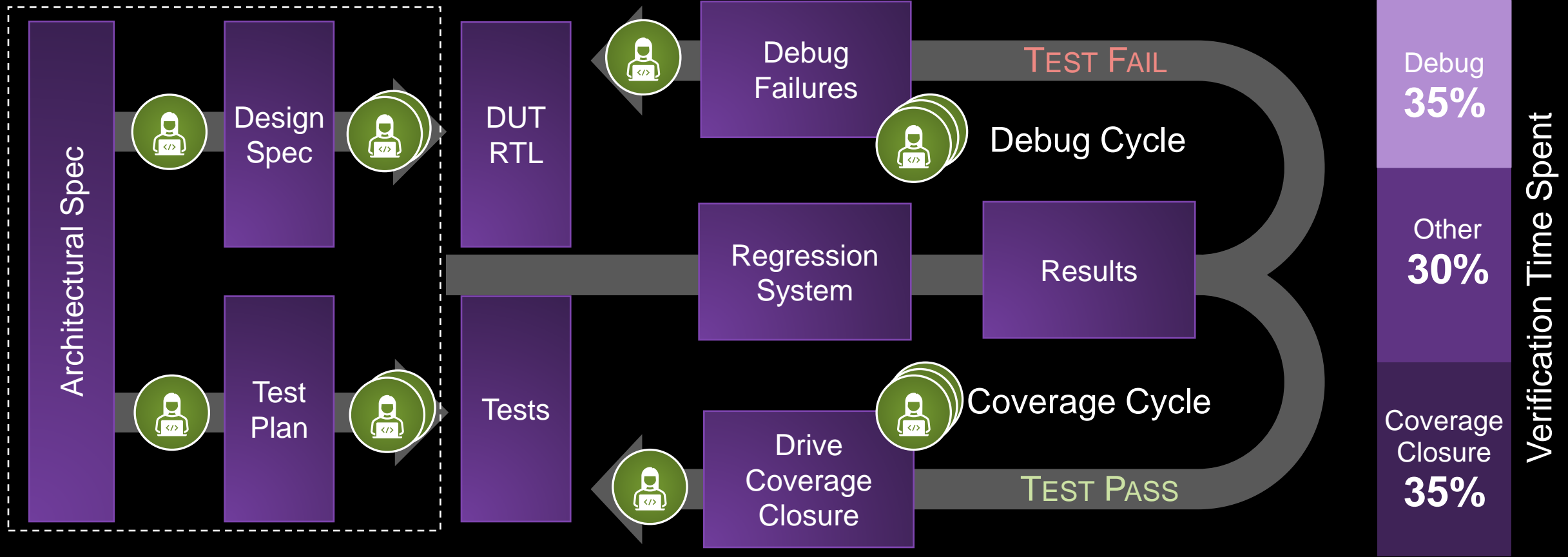
NextGen GUI

- Intuitive Search
- Screen-Friendly Font
- User Selectable Modes
- Clean Appearance

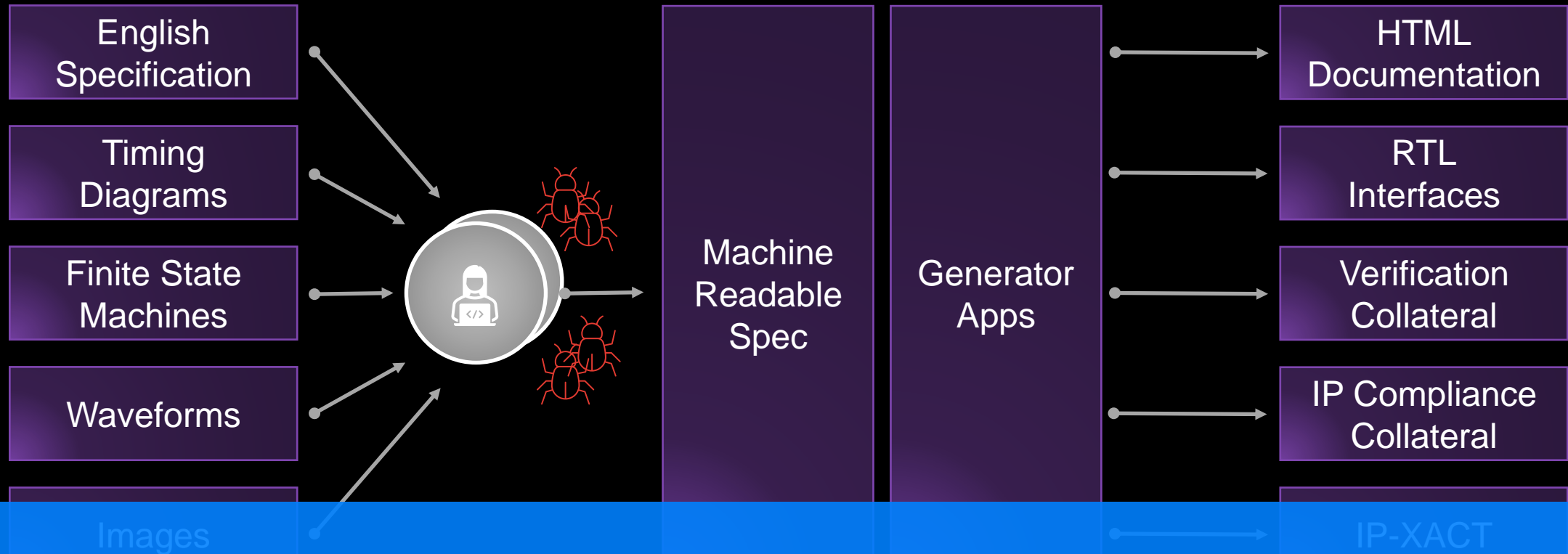
Apps, Analytics, API

- Unified Database & Server

What About Specification Automation?



Typical Specs → Collateral Flow



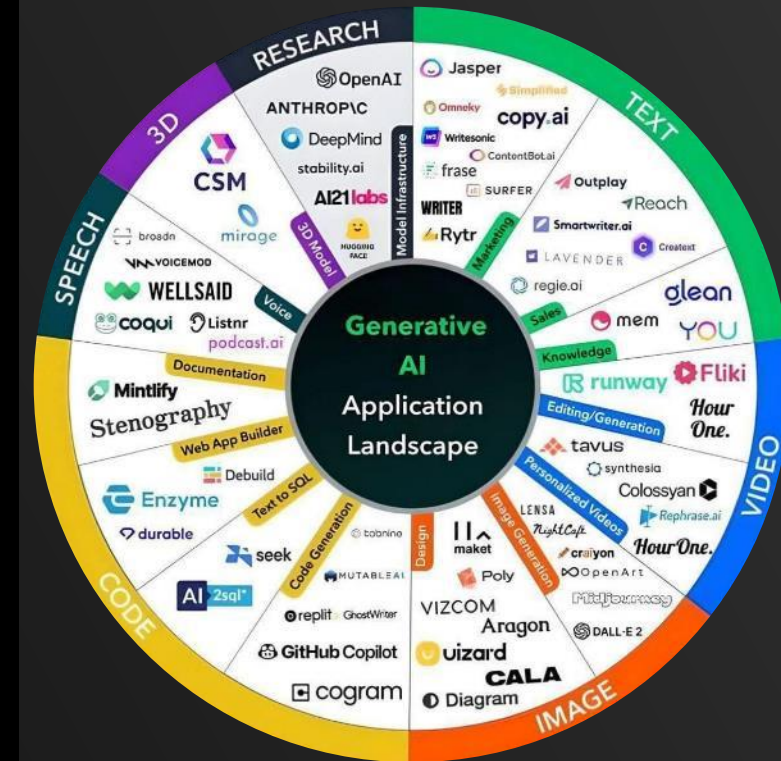
Generative AI Can Help to Remove Ambiguity & Provide Automation.

Introduction to Generative AI

- Generative AI: a branch of AI used to create new content, including audio, code, images, text, simulations, and videos.
- Recent advances in GPT (Generative Pre-trained Transformer) technology have enabled applications like ChatGPT
- ChatGPT is an LLM interface that can converse with a human, write essays, create websites automatically etc.

If Generative AI can create “intelligent” responses, can it write Verilog, automate chip design flow, and create layouts?

LLM Application Landscape



How about EDA?

RTL Copilot

Natural Language Text → SystemVerilog Code

DV Assistants with Engineer in the Loop

```
10 /* Design a decade counter that counts from 0 through 9, inclusive.
11  * On the positive edge of the clock:
12  * if reset is high, reset the output q to 0.
13  * Otherwise, only increment the output q if the slowena input is high and q is not 9.
14  */
15 module count_slow(input clk, input slowena, input reset, output reg [3:0] q);
16
17 AI proposal 0:
18 AI proposal 1:
19 AI proposal 2:
20
21
22
23
24
25
26
27
28
29
30
```

```
...
module count_slow(input clk, input slowena, input reset,
output reg [3:0] q);
always @(posedge clk) begin
if (reset == 1'b1)
q <= 4'd0;
else
begin
if (slowena == 1'b1 && q != 4'd9)
q = q + 4'd1;
end
end
endmodule
...
```

Press Ctrl+Space to show Template proposals Press 'Tab' from proposal table or click for focus

Provide Spec in
Natural Language

Use LLM interface to
Generate RTL code

Review Code

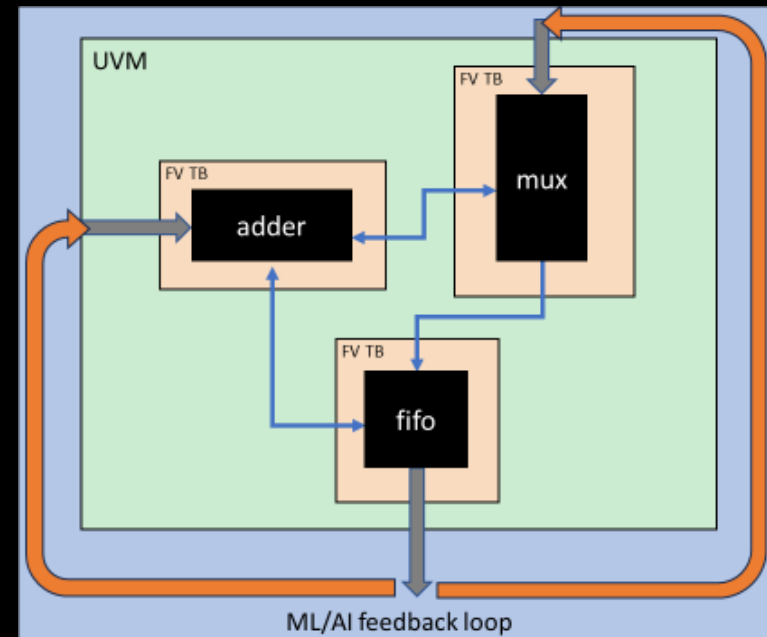
Accept / Reject

Generative AI Vision TechTalk

Presented by Microsoft (Eric Berg) at DAC 2023

HW Vision

- Generate RTL modules (adder, mux, fifo)
- Generate Formal Verification Testbench (FV TB) for design exercise
- Generate connection logic
- Generate UVM TB for connected block
- Optimize random test stimulus using ML/AI tools



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Generative AI Promises

**Transform English
Specification
to Machine Readable
Specification**

**Multi-Step
Reasoning
Assistant**

**Code
Advisor**

**Test Collateral
Generation**

Generative AI: Key Challenges



**Reinforcement Learning with Human Feedback
& EDA Tools as Agents in the Loop can help**

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The Human controls the scope of Verification

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Question to DALL-E

Show the Level 5 vision of Autonomous Verification



Robots Doing Verification



We Focusing on What's Important

Thank You