



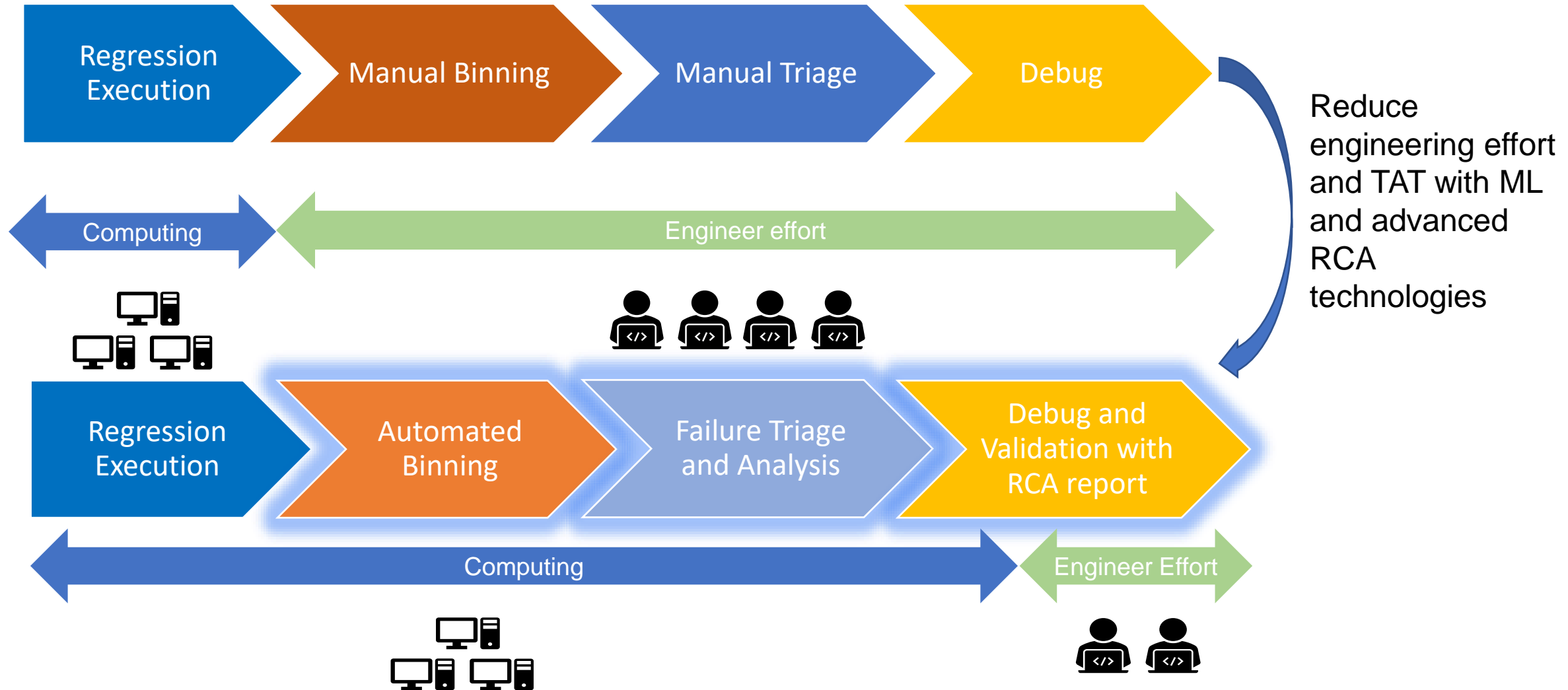
Debug Automation with AI

Craig Yang, Jaw Lee, Sherwin Lai
Verdi R&D, Synopsys Taiwan

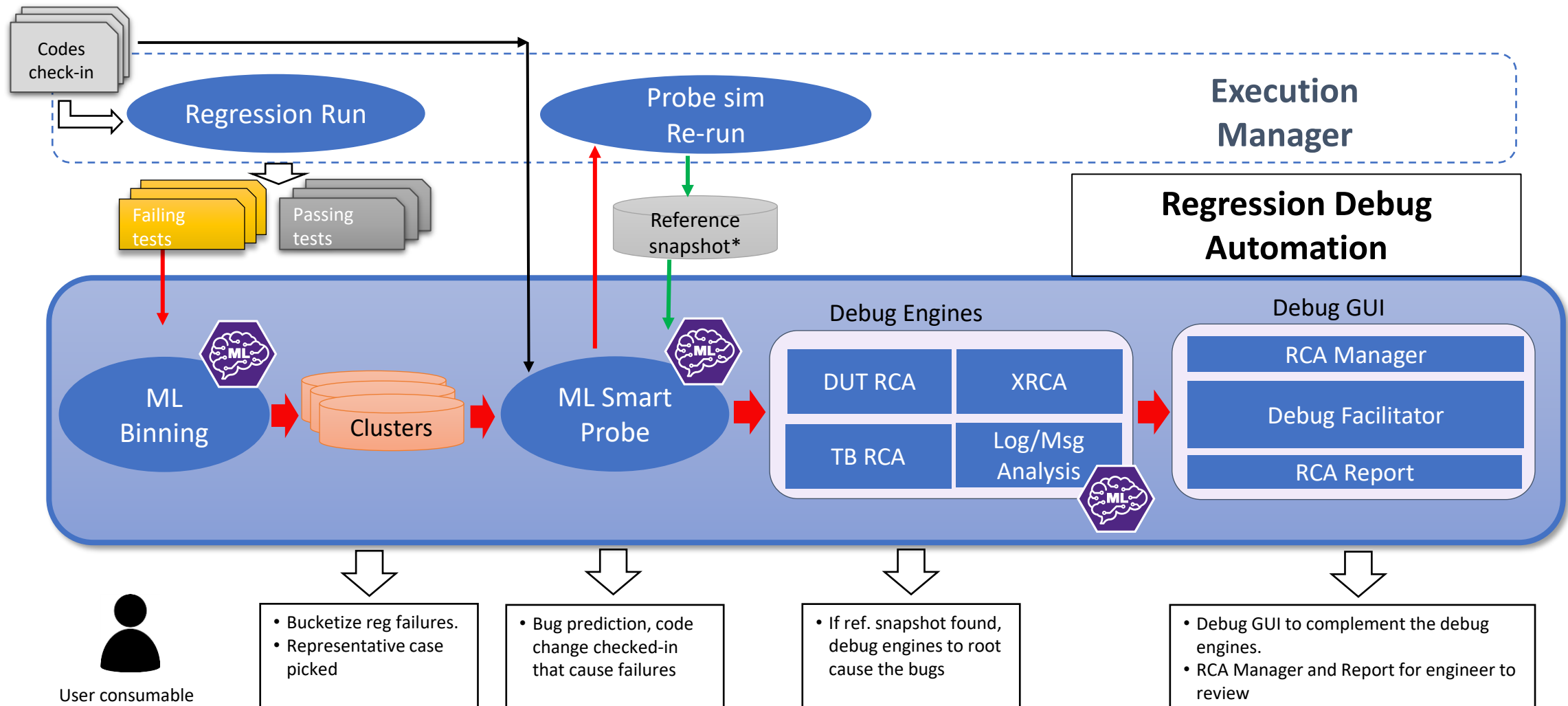


Motivation and Debug Flow

Regression Debug Automation Motivation



Regression Debug Flow with ML

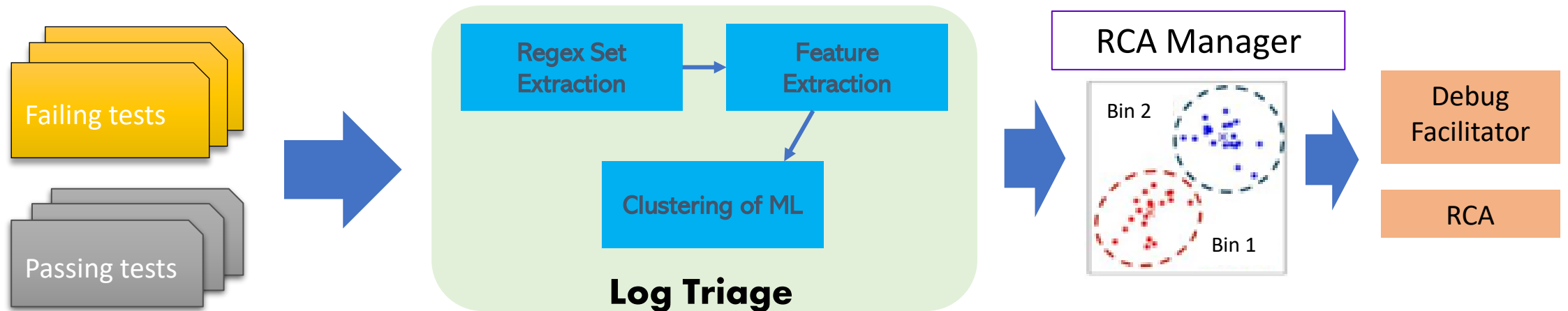


Regression Binning

Regression Binning with ML

- Apply machine learning technology for regression binning
 - Perform failure clustering based on the similarity of simulation logs

Regression Binning Engine



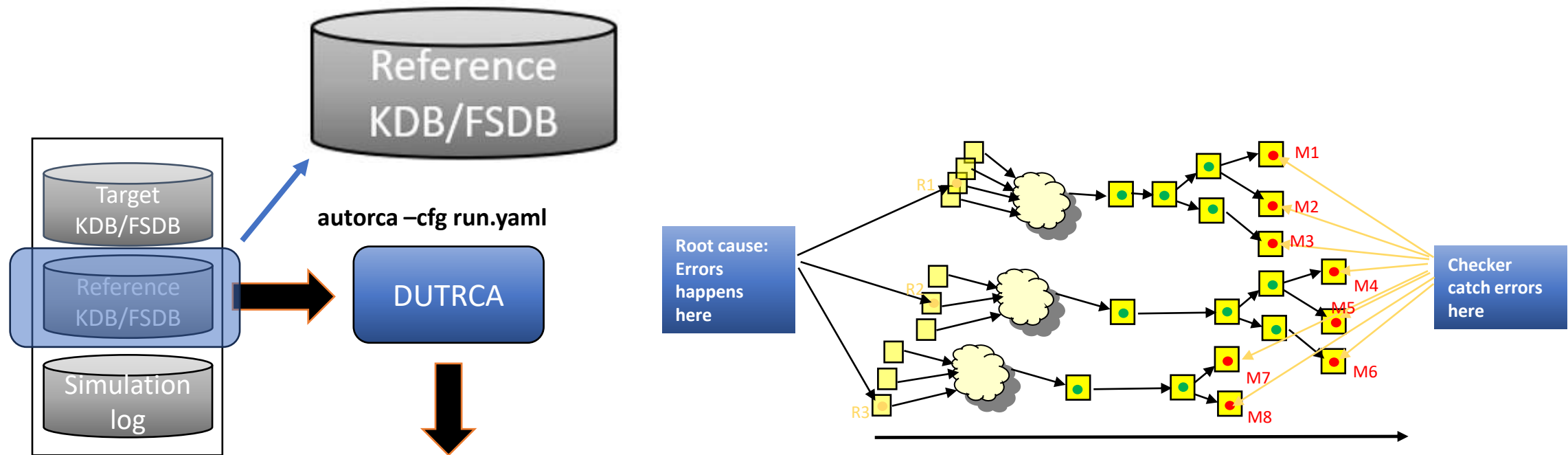
Useful Regression Binning Features

- Predefined Errors
 - UVM Errors, OVM Errors, SVA Failures, etc.
- User Defined Errors
 - Control the Message Chosen Mechanism
 - Filter Rules
 - Waive Rules
 - Rule Priority
 - Adjust the Binning Result
 - Replace Rule
 - Pass Rule
- Multiple-Error Binning

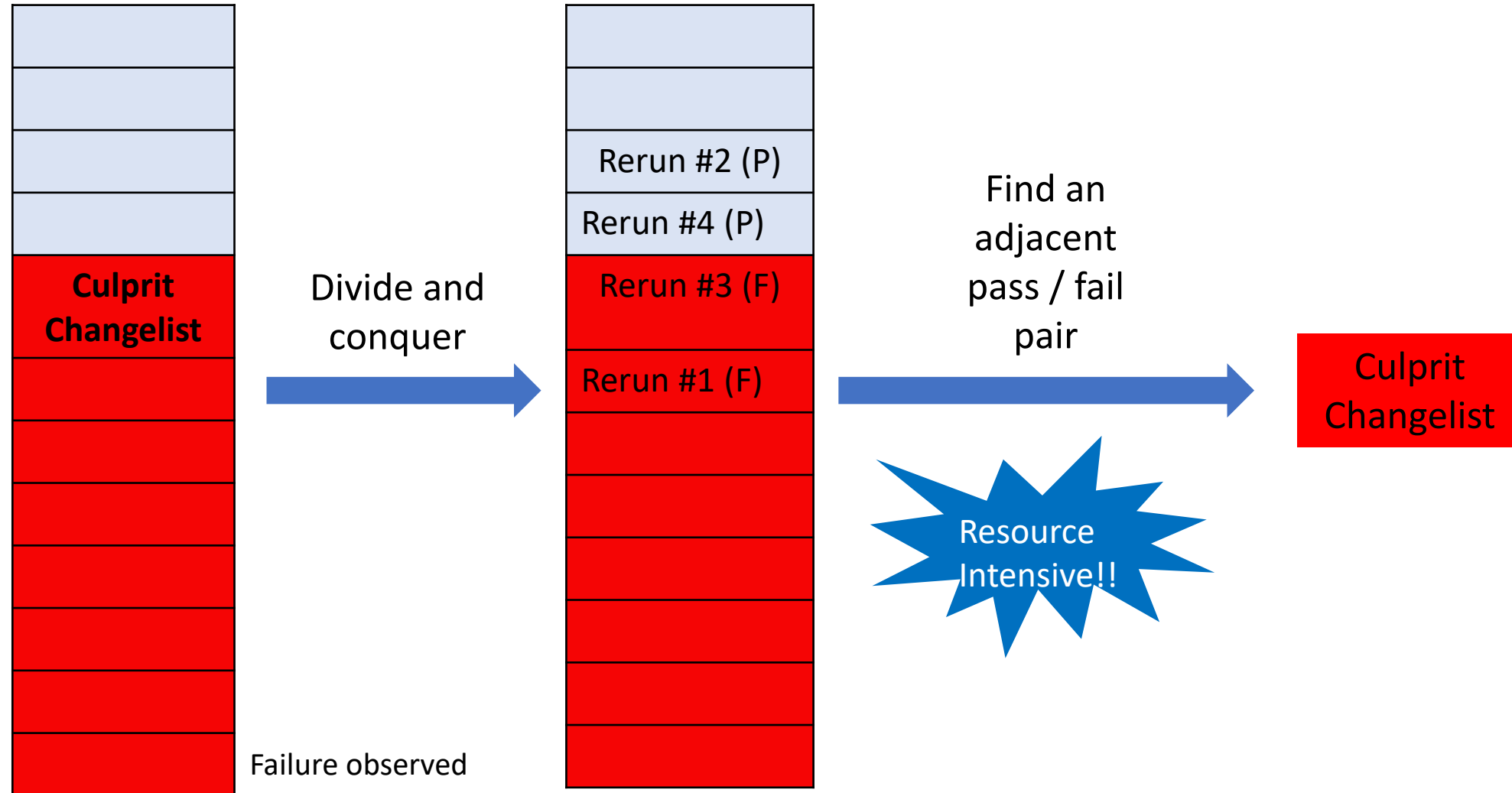
Bug Prediction

Probe Engine

- Some debug engines need a reference design snapshot
- We need a probe engine to find the reference design snapshot

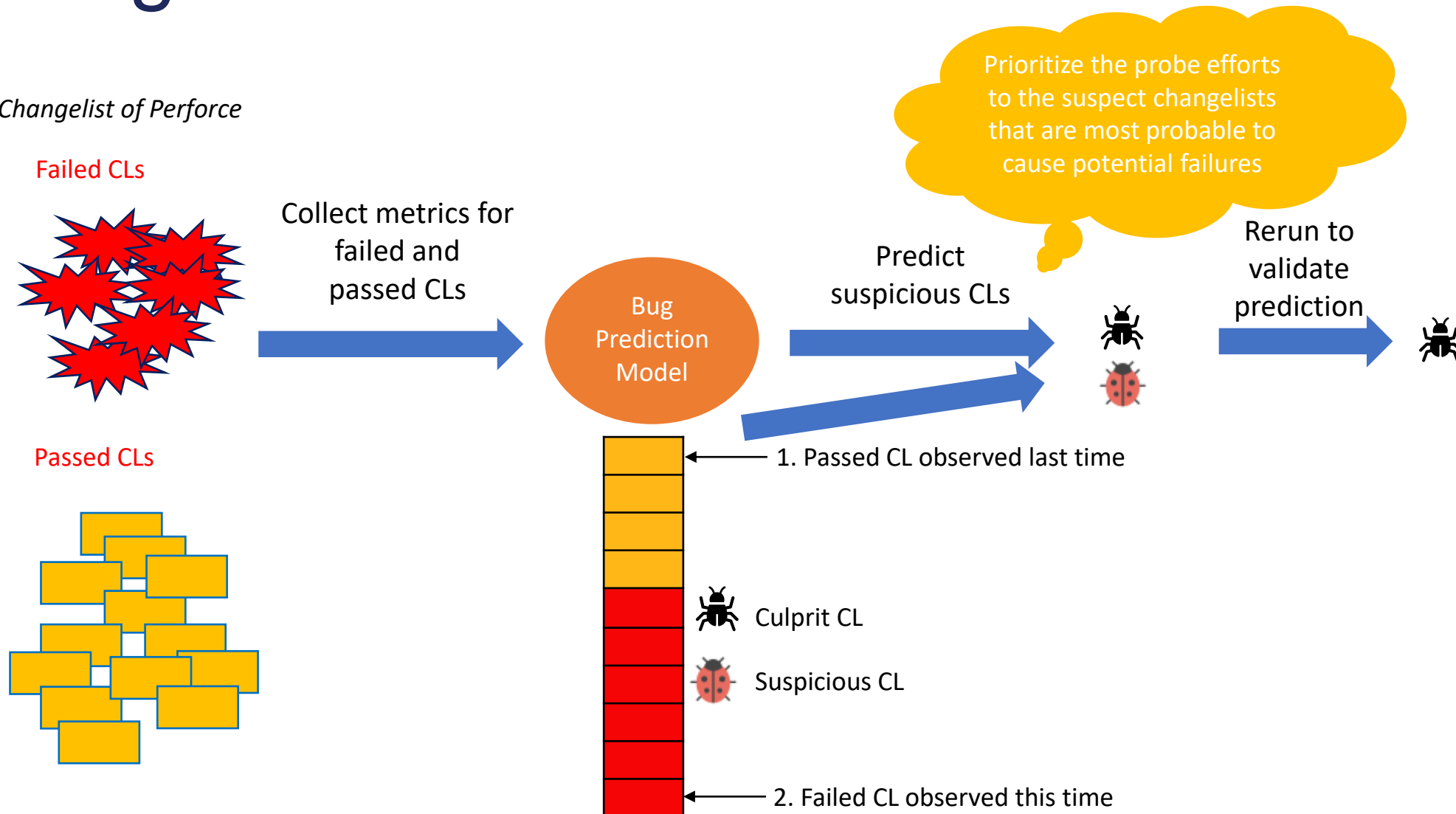


Traditional Probe without Bug Prediction



Bug Prediction

CL: Changelist of Perforce



Bug Prediction for Smart Probe

- Prioritize the probe efforts to high-risk changelists

<rcaSmv:1> rda_report.json (on odclegacy0136)

File View Tools Window Help Menu

Total 2 Failed Bucket(s), 2 Failed Case(s)

Bucket	Action
Summary	
pass (0)	
uvm_error:fail (2)	
Bucket1 (1 Fail)	
/remote/vgrnd10/tsyang/test/lab-RDA_SmartProbe_eman_byLien/03_add_test_run_dir/work/rca.work/...	
Original Case:/remote/vgrnd10/tsyang/test/lab-RDA_SmartProbe_eman_byLien/03_add_test_run_d...	
Error Message:UVM_ERROR ./Design/design/Testbench/src/minsoc_tb/ethernet/eth_driver.sv(72) @ 4000740: uvm_test_top.env.eth_i_agent.driv [eth_driver] Wrong preamble data to drive.	
Remaining Cases	
Bucket2 (1 Fail)	
/remote/vgrnd10/tsyang/test/lab-RDA_SmartProbe_eman_byLien/03_add_test_run_dir/work/rca.work/...	
Original Case:/remote/vgrnd10/tsyang/test/lab-RDA_SmartProbe_eman_byLien/03_add_test_run_d...	
Error Message:UVM_ERROR ./Design/design/Testbench/src/minsoc_tb/minsoc_scoreboard.sv(405) @ 4361860: uvm_test_top.env.sb[uart_scoreboard] DCE_TX_DCE_RX_COMP : Fans Data Mismatch between dce_tx value is 10100101 and dce_rx value is 1011001	
Remaining Cases	

Probe Summary Details (on odclegacy0136)

```
[Probe] Info. time_out_in_minutes : 1430
[Probe] Info. #####
[Probe] Info. Failed tests to be probed : build/eth_test
[Probe] Info. Failed tests to be probed : build/uart_test
[Probe] Info. Get all changeLists from 2023/01/15:10:22:47 to 2023/01/16:10:22:47
[Probe] Info. p4 -p localhost:6487 -c labRDA_tsyang_eb3be2f21667460ccc492028125c886e changes -s submitted @2023/01/15:10:22:47,2023/01/16:10:22:47
6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 |
22 | 23 | 24 | 25 | 26 | 27 |
[Probe] Info. eman -regr_config /remote/vgrnd10/tsyang/test/lab-
man_byLien/03_add_test_run_dir/work/eman_out/probe_work_dir_2023-03-07_fff980e03c/probe.emc -local_host -no_debug_rerun -disable_end
[Probe] Info. ChangeList 6 has risk: 0.330000
[Probe] Info. ChangeList 7 has risk: 0.480000
[Probe] Info. ChangeList 8 has risk: 0.540000
[Probe] Info. ChangeList 9 has risk: 0.360000
[Probe] Info. ChangeList 10 has risk: 0.290000
[Probe] Info. ChangeList 11 has risk: 0.390000
[Probe] Info. ChangeList 12 has risk: 0.220000
[Probe] Info. ChangeList 13 has risk: 0.980000
[Probe] Info. ChangeList 14 has risk: 0.030000
[Probe] Info. ChangeList 15 has risk: 0.450000
[Probe] Info. ChangeList 16 has risk: 0.340000
[Probe] Info. ChangeList 17 has risk: 0.350000
[Probe] Info. ChangeList 18 has risk: 0.230000
[Probe] Info. ChangeList 19 has risk: 0.460000
[Probe] Info. ChangeList 20 has risk: 0.010000
[Probe] Info. ChangeList 21 has risk: 0.020000
[Probe] Info. ChangeList 22 has risk: 0.120000
[Probe] Info. ChangeList 23 has risk: 0.360000
[Probe] Info. ChangeList 24 has risk: 0.440000
[Probe] Info. ChangeList 25 has risk: 0.150000
[Probe] Info. ChangeList 26 has risk: 0.290000
[Probe] Info. ChangeList 27 has risk: 0.370000
[Probe] Status. ##### Start Probing #####
[Probe] Info. p4 -p localhost:6487 -c labRDA_tsyang_eb3be2f21667460ccc492028125c886e sync @10
```

Invoke Probe Summary

Probe Summary Details (on odclegacy0136)

Probe Summary	
Remark	bucket1 test passed in changelist 12 but failed in changelist 13
Target Changelist	13
Reference Changelist	12

Open Probe Log OK

Bug Prediction for Risk Assessment

- Help the users assess high-risk changelists without running probe

The screenshot displays a software interface with a main window titled '<rcaSmv:1> rda_report.json (on odclegacy0136)'. A 'Changelist Risk' dialog box is open, showing a table of changelists with their risk scores and descriptions. A 'Changelist Details' dialog box is also open, providing more information about a specific changelist.

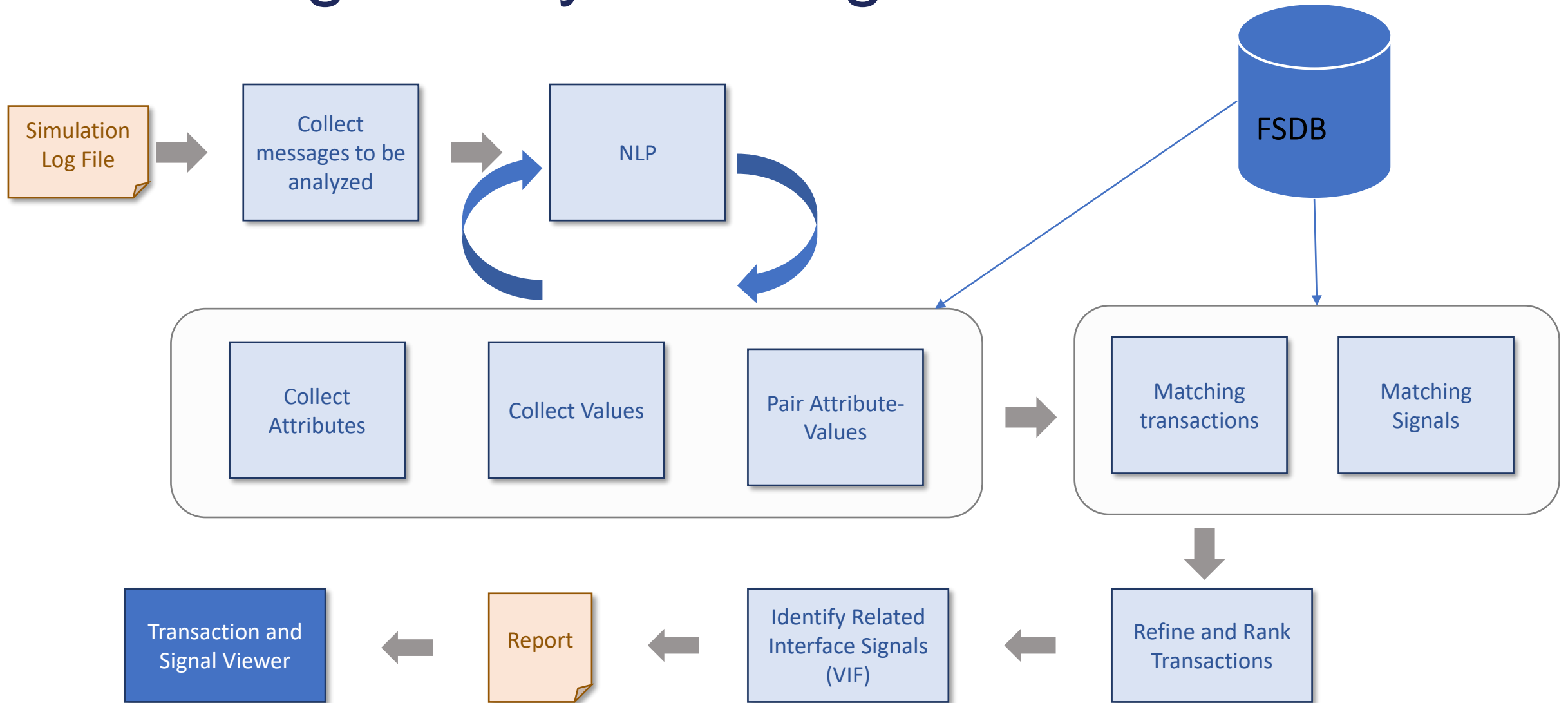
Changelist	Risk	Description
1 7676237	0.77	Fixed the issue at 32G was not moving to LOCKED
2 7679189	0.74	Fix IDE Base Seq. configured EP VIP to initiate a me
3 7665999	0.74	Fix for en code_collab_id:139
4 7667358	0.65	Reverti parity test code_collab_id:139
5 7664602	0.64	Gen6: Fixed to Rcvr.Lock from L0 in the middle
6 7663573	0.63	Gen6 Redo EQ Te Redo EQ from lo
7 7677463	0.61	Fixed pack/unpack EP bit in dword1. bit 15.

Changelist Details (on odclegacy0136)

Changelist Info	
Changelist	7676237
Date	2022/06/16 11:02:42
User	kumard@kumard_pcie_svt_pcie_dev_30_April_2018
Message	Fixed the issue moving to LOCKED state from ALIGN RxBlockAlign w

Message Analysis

Message Analysis – High Level Flow



Message Analysis – Example

```

TBAR_INFO: Started analyzing debug message(s) from simulation log file {/remote/vgsource12/ikshvaku/TD.VERDI_REG/unit_VERDI/unittest/evProds/tbAutoRCA/testData/swayCases/TB_ERRORR/out_230/examples/simv.log}
TBAR_INFO: Simulation log file contains ERRORS(14) debug messages.
TBAR_INFO: Analyzing the first ERROR log message.
TBAR_INFO: Analyzing the below log message.
           {UVM_ERROR ubus_example_master_seq_lib.sv(206) @ 80: uvm_test_top.ubus_example_tb0.ubus0.masters[1].sequencer@loop_read_modify_write_seq.rmw_seq [read_modify_write_seq]
loop_read_modify_write_seq.rmw_seq Read Modify Write Read error!}
TBAR_INFO: Completed analyzing debug message(s) from simulation log file.
TBAR_INFO: Matching attribute/values are listed below.
TBAR_INFO: {addr:020a}, {data[0]:e9}
TBAR_INFO: Matching transactions after analyzing actual, next and previous messages are listed below
TBAR_INFO: Stream: {$trans_root/uvm_test_top/ubus_example_tb0/ubus0/masters[1]/driver/seq_item_port} Matching transactions: {2}
TBAR_INFO: Stream: {$trans_root/uvm_test_top/ubus_example_tb0/ubus0/masters[1]/sequencer} Matching transactions: {1}
TBAR_INFO: Total matching transactions {3}
TBAR_INFO: Matching virtual interface paths are listed below
TBAR_INFO: /ubus tb top/vif Signals: {sig read,sig write,sig addr}
TBAR_INFO: Top ranked transaction details are listed below
TBAR_INFO: Transaction {get_next_item(req)[80-80]} Stream {$trans_root/uvm_test_top/ubus_example_tb0/ubus0/masters[1]/driver/seq_item_port} Component type {uvm_driver} Port type {uvm_seq_item_pull_port}
TBAR_INFO: Connected to {uvm_test_top.ubus_example_tb0.ubus0.masters[1].sequencer.seq_item_exp0rt} Component type {uvm_sequencer} Port type {uvm_seq_item_pull_imp}
TBAR_INFO: Please run the {/slowfs/vgvips19/prasadtc/verdiLog/tbAutoRCA/reports//simvErrorAnalysisLog/run_verdi} script to view the simv log file analysis results in Verdi.
    
```

Larger set of transactions

Smaller set of Related transactions

The screenshot shows the Verdi tool interface. The top window displays a hierarchy of components on the left, a timeline of transactions in the center, and a details pane on the right. The bottom window shows analysis details for a specific transaction, including matching attributes and a simulation log message.

Interested transaction attributes

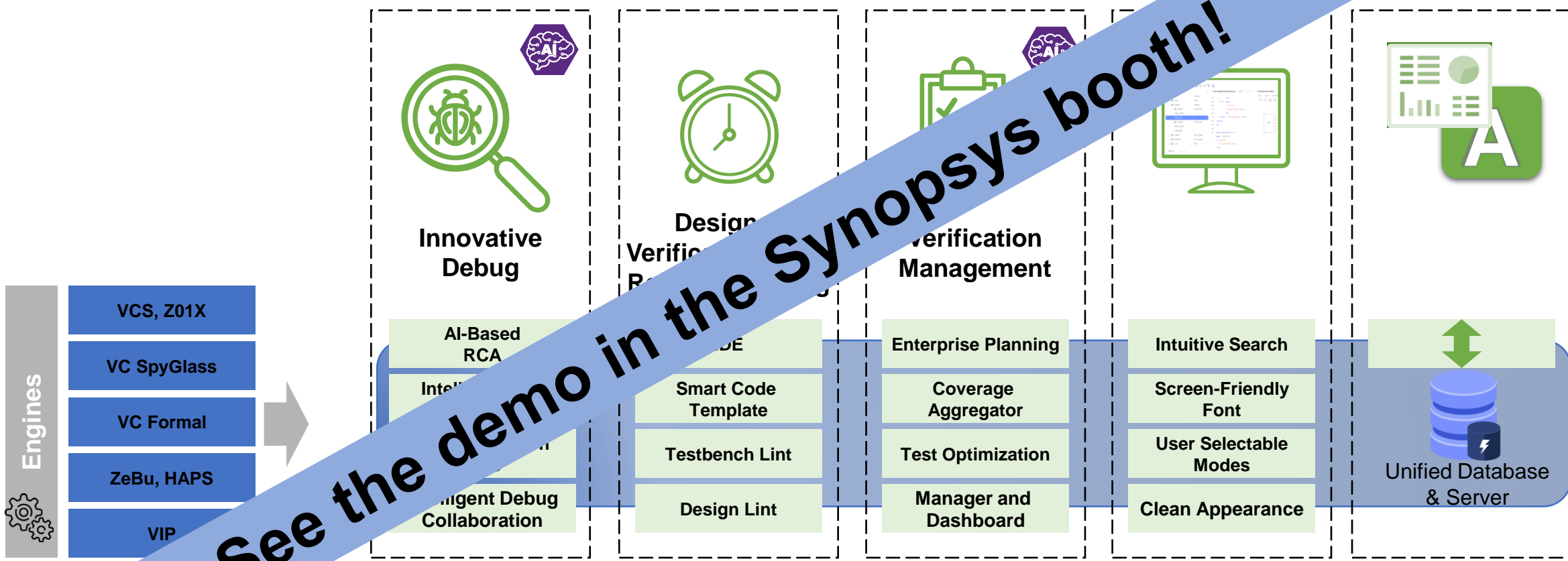
Matching transaction details

Simulation log message

Summary

- Manual regression debug is tedious, but we can automate it with AI and advanced RCA technologies
- **Regression binning** classifies many failed tests into a few bins of different errors
- **Bug prediction** reduces the time on locating reference snapshots for debug engines
- **Message analysis** identifies transactions and VIFs that are related to the error message

Introducing Next-Generation Verdi Platform



Questions