Empowering Innovation in Logic Verification

Harnessing collective wisdom across tools, processes, and people

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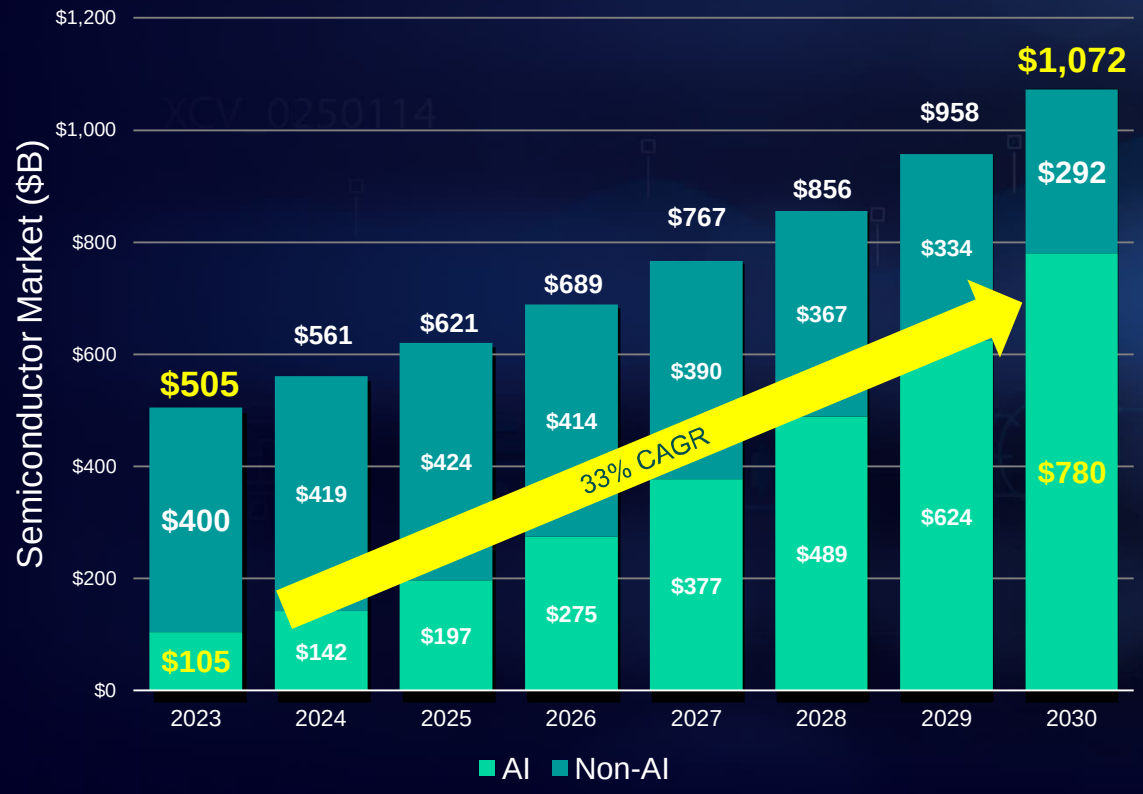
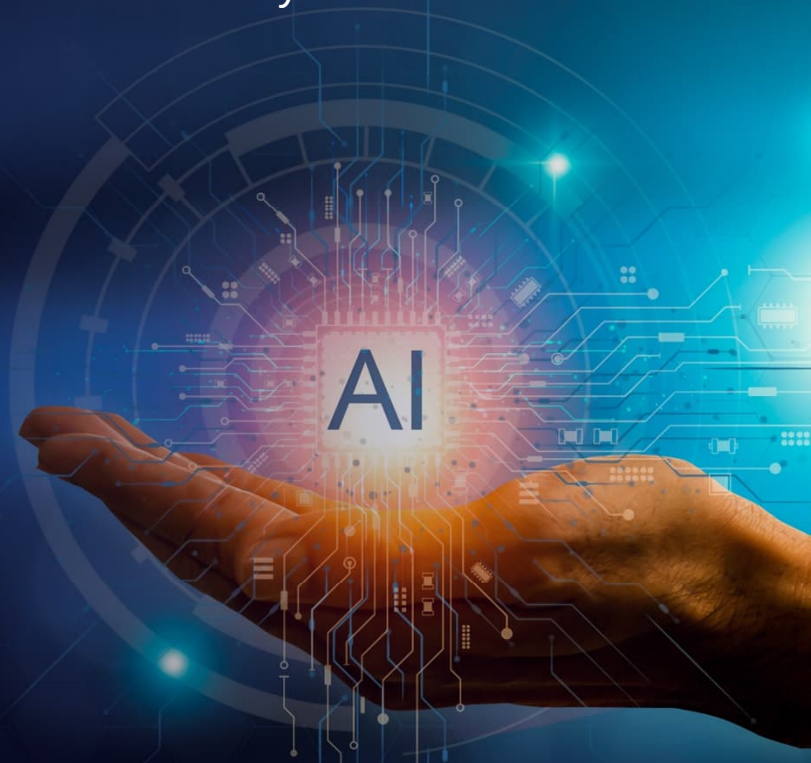
Total Semiconductor Market and AI Semiconductor Market

In 2023 21% of semiconductor market associated with AI and grows to 73% by 2030





Source: IBS Jan 2024 Report: First Generative AI Report: Impact of Generative AI on Semiconductor Industry

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Disruptive trends in the global datasphere

Reshaping computing, networking, communication, security, and applications

1^{ZB} = 1,000,000,000,000,000,000,000 (10^{21}) = 250 billion DVDs

Global Datasphere is a measure of how much data is created, captured, replicated, and consumed each year.

Source: IDC Apr 2023 Report: Worldwide IDC Global Datasphere Forecast, 2023-2027

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Macro trends in growing complexity

Reshaping computing, networking, communication, security, and applications

Sensors /
Edge Computing

Collect

5G /
Wireless

Transmit

Cloud /
Networking

Process

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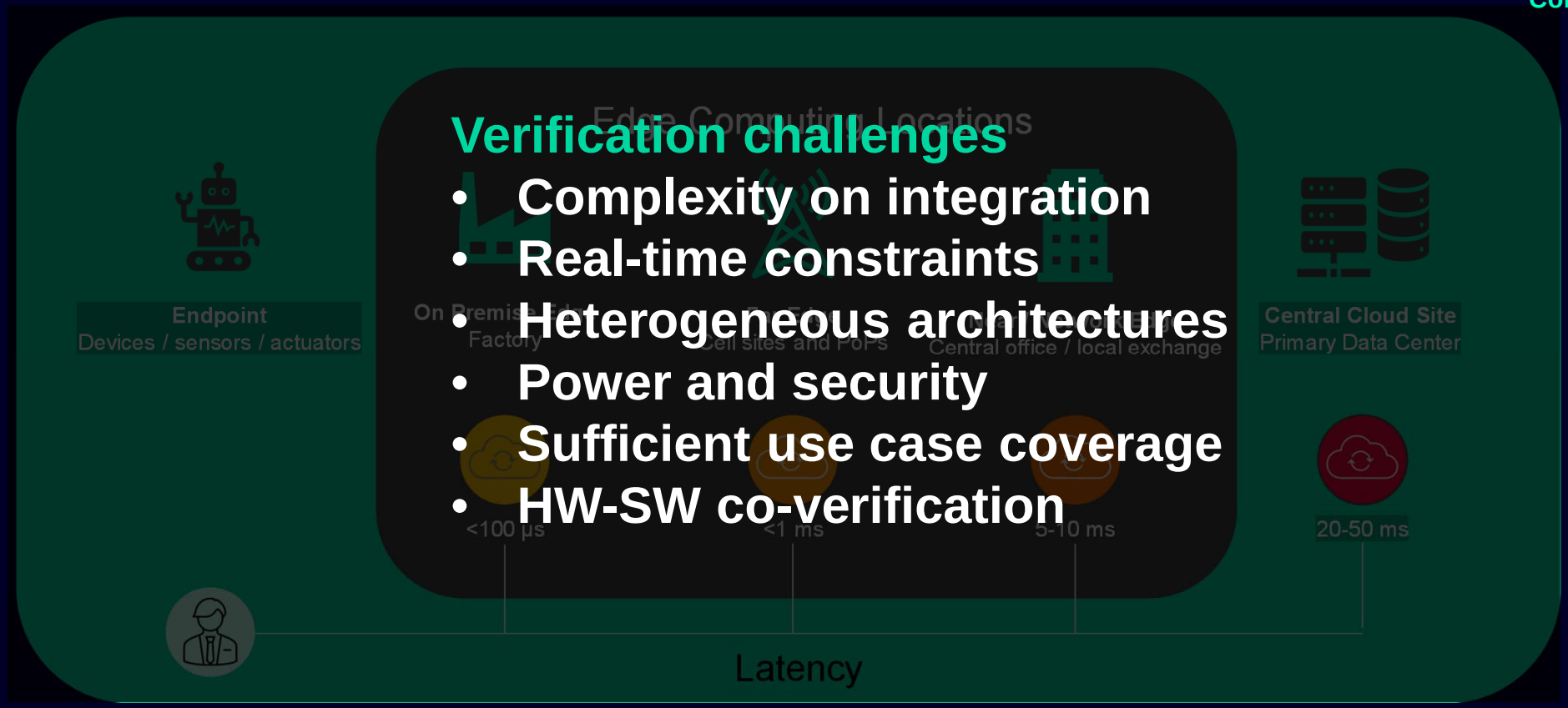
Edge computing trends — it's all about latency!

75% of data compute moves to the edge in the next few years

Collect



Verification challenges

- **Complexity on integration**
- **Real-time constraints**
- **Heterogeneous architectures**
- **Power and security**
- **Sufficient use case coverage**
- **HW-SW co-verification**

Source: Application PerformancemArticles, Digital Experience, Network Performance, Mar 24, 2022
AXIOS, AI drives explosion in edge computing, Feb 16, 2024

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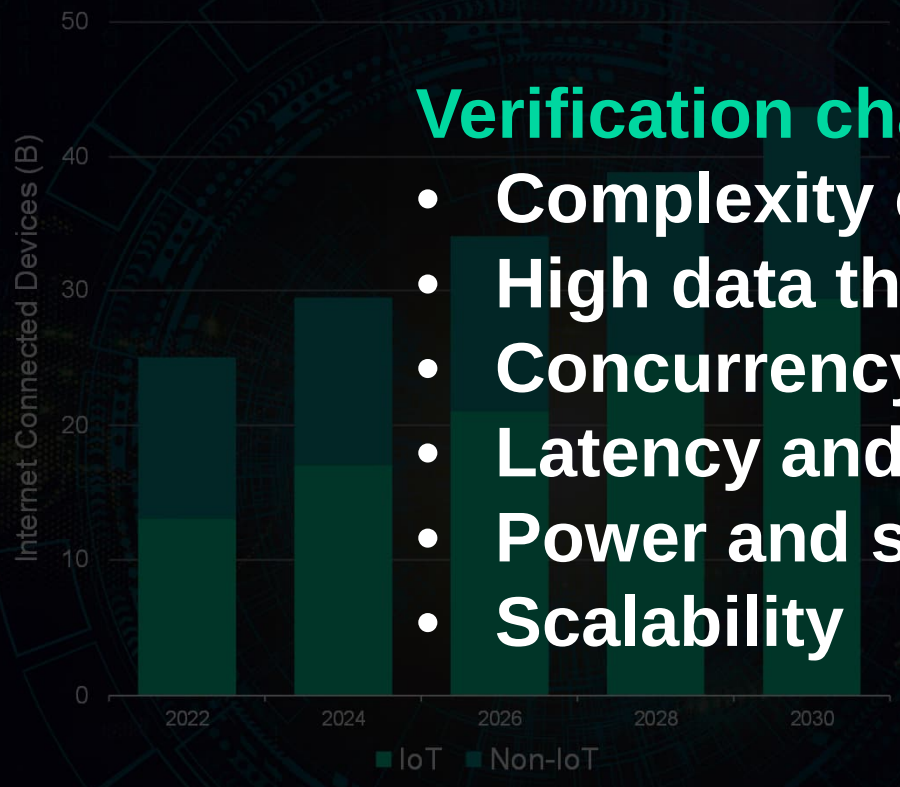
Hyperconnected world by 2030

44 billion devices connected to the internet by 2030, growing at a 12% CAGR

Transmit



Verification challenges includes

- **Complexity of interconnections**
- **High data throughput**
- **Concurrency**
- **Latency and timing**
- **Power and security**
- **Scalability**

World population 8.5 billion by 2030
44 billion internet devices by 2030

- WiFi 6 improved performance, capacity, battery life, speed in congested areas
- 5G high speed, low latency, massive capacity

- *Cyber security & resilience an issue, and AI critical to monitoring and preventing issues*
- *AI becomes more critical to manage, optimize, and debug networks*

Source: Exploding Topics: Number of IoT Devices (2024), Feb 19, 2024

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Hyperscale computing — it's all about scalability!
Cost-effectiveness, high performance, reliability and resilience, support big data

Process

Verification challenges includes

- Immense scale
- Stringent performance
- Power requirements
- Complex concurrency
- Robust security and reliability

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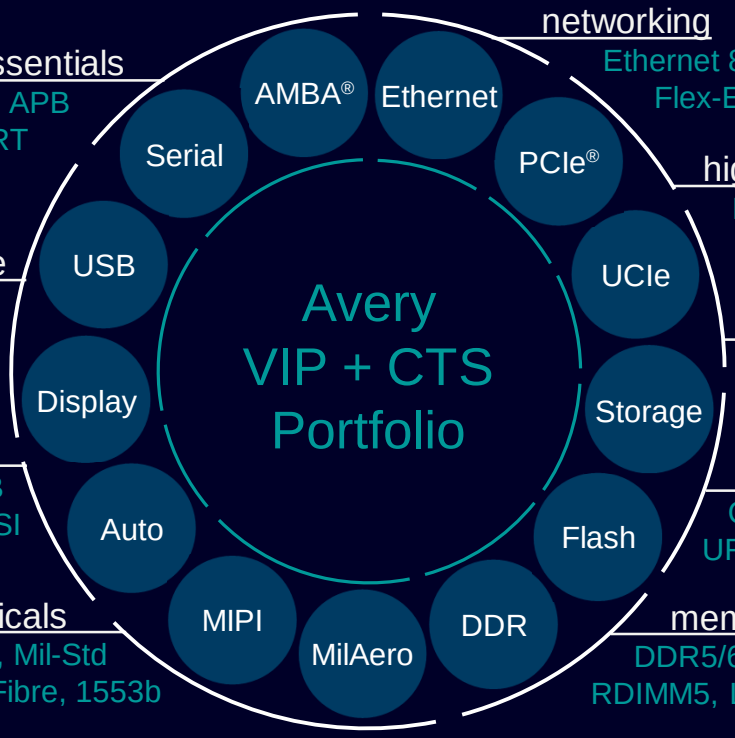
Accelerated Confidence from Siemens EDA – Avery Verification IP broad portfolio

Accelerated

- First To Market AND high quality via partnerships
- Fast standard SV/UVM runs on all engines
- Supports QEMU co-simulation for HW/SW co-dev
- Sim Acceleration on emulator and prototype system

Confidence

- Tested on multiple controller designs from IP Partners
- Finds bugs in design IPs that other VIPs miss
- Future-proof Roadmap and Packaging
- Broad Portfolio: Verification IPs + Compliance Tests



networking
Ethernet 800G/1600G, MacSec
Flex-E, BaseT, UEC, Infiniband

high-perf compute
PCIe5/6/Gen7 interconnect
CCIX, CXL 2.0/3.0/3.1

3DIC/chiplet
UCIe 1.1/2.0, HBM2E/3/4
Custom Solutions & Services

high-perf storage
CXL2/3, NVMe, UAS, SAS, SATA, AHCI,
UFS4, eMMC, SD, ONFI, Flash/SSD stds

memory models
DDR5/6, LPDDR5/6, GDDR6/7, DFI
RDIMM5, LRDIMM5, NVDIMM5, HBM4

mil-aero verticals
PCI, JESD204, SRIO, Mil-Std
SpaceWire, SpaceFibre, 1553b

automotive net
10M-1G T1 Auto Ethernet, TSN/AVB
CAN/LIN, Flexray, MIPI CSI/DSI

human interface
USB4, USB3.2, PD, SoundWire
HDMI2.1a, DP2.0, DPI, SFPDP

SoC essentials
CHI, ACE5, AXI5, AHB, APB
CXS, TileLink, JTAG, UART
SMBus, SPI/xSPI, I2C/I3C/I2S

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Accelerated Confidence from Siemens EDA – Avery Compliance Test Suites find bugs!

Accelerated

- First To Market AND high quality via partnerships
- Fast standard SV/UVM runs on all engines
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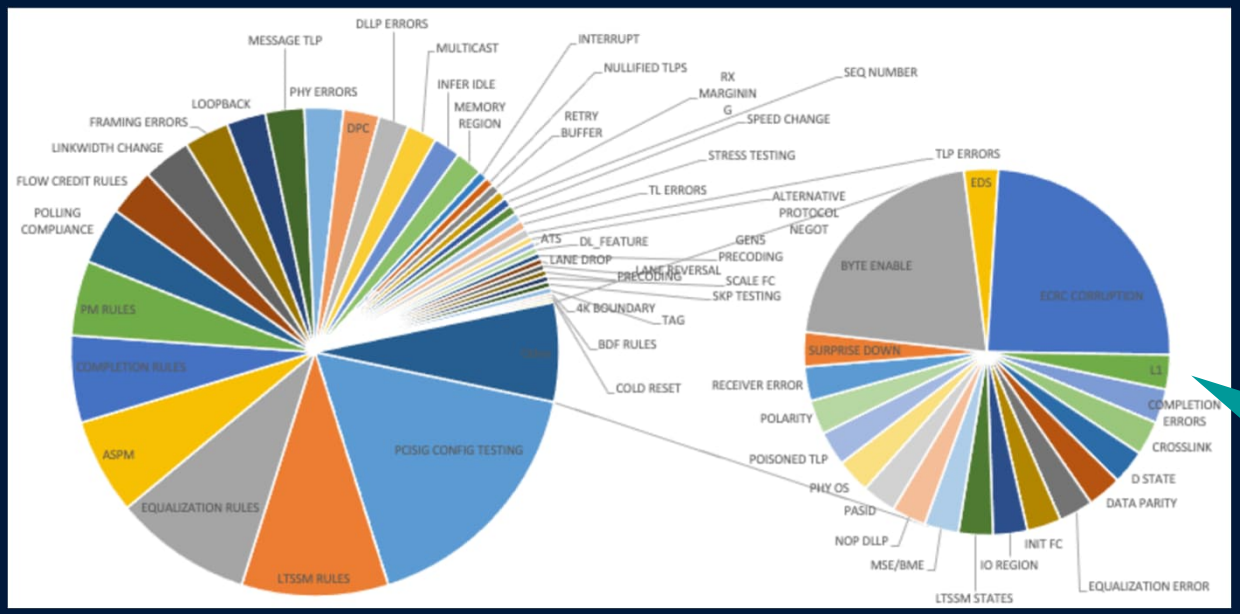
Build vs Buy? Rely on Avery VIP+CTS for compliance/quality, freeing up your resources



Avery Compliance Test Suites:

- Covers whole spec, not just std tests
- Constrained-random SV/UVM code
- Full test plan and coverage model
- Still finding PCIe5 bugs in IP configs
- **The industry's signoff VIP / test suite**

"you found an IP bug the IP vendor VIP did not catch – with just ONE test"
– HPC customer

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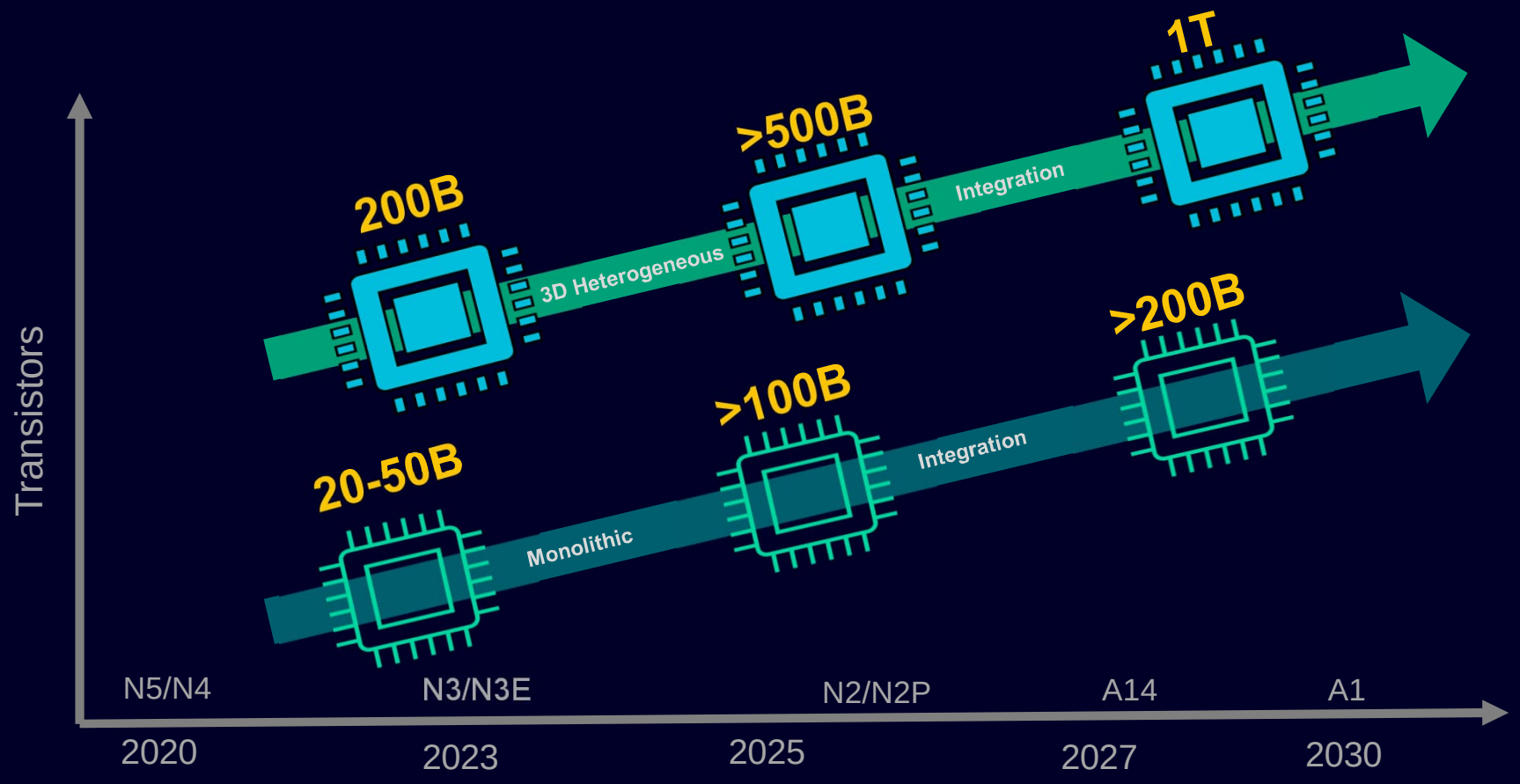
Chiplets and 3DIC

Moving monolithic SoCs to 3DIC and chiplet-based design



Source: WCCF Tech, TSMC Aims to Integrate Over 1 Trillion Transistors, Dec 2023

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Chiplets and 3DIC

Moving monolithic SoCs to 3DIC and chiplet-based design

Cost-effective scaling

- Alternative to traditional Moore's Law scaling through higher integration

Enhanced performance

- Increases processing power and speed by reducing interconnect

Reduce power consumption

- Shorter interconnects reduce power loss and improve energy efficiency

Interconnect protocol challenges

- Verifying that complex interconnect protocols adhere to specification
- Verifying compatibility between different chiplets from various vendors or design team

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Why do we need UCIe and how do we deal with that complexity?

Moving from a simple “wire” to a complex managed die-to-die protocol “smart wire”

Building a standards-based chiplet ecosystem:

Flexible: Highly configurable Interconnect

- **package, modules, protocols, flits modes**

Native: built-in support for PCIe/CXL flit format

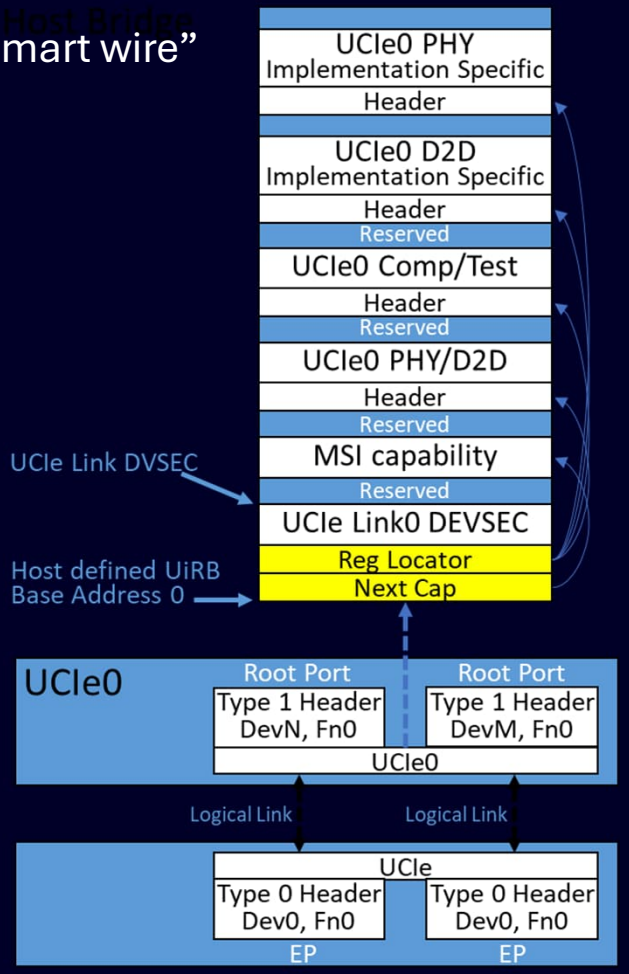
- **leveraging PCIe/CXL software stack**

Inclusive: other protocols over streaming mode

- **Example: AXI, CHI, CXS**

Expandable: retimer support

- **Enable off-package electrical/optical link**



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UCIe comes of age with the UCIe 2.0 specification (August 2024)

Adds manageability architecture, debug and test support, sideband extensions, 3D PHY

- **UCIe Manageability Architecture**
  - **Management Transport Protocols**
    - **UCIe Memory Access Protocol (UMAP)**
    - **UCIe Test and Debug Protocol**
    - **Vendor Defined Protocol**
  - **Management Transport Packet**
  - **Management Capability Structure**
- **UCIe Debug and Test (DFx) Architecture**
  - **Utilizes Manageability Infrastructure**
- **X8 Standard Package Support**
- **Sideband Feature Extensions (SBFE)**
  - **Sideband-only (SO) Port**
  - **Sideband Performant Mode Operation (PMO)**
- **UCIe-3D PHY**

Our statement of support in the UCIe2.0 launch on Aug 6 2024:

"Building on our leadership in chiplets technology and ....

With our UCIe2.0 Verification IP and Compliance Test Suite solutions, Siemens continues its UCIe design verification leadership.

And because version 2.0 of the UCIe standard incorporates advances that support mainstream design for test (DFT) practices, it paves the way for next-generation products capable of fully leveraging Siemens' industry-leading Tessent software."

Mike Ellow, CEO of Silicon Systems for Siemens EDA

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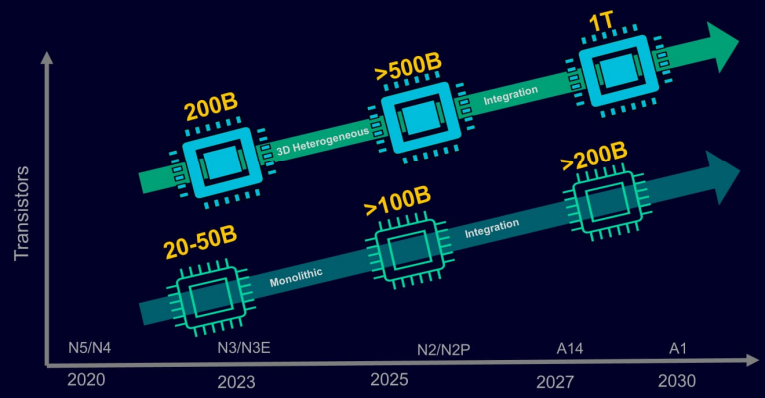
Software defines and differentiates successful products
Development & validation must start as early as possible

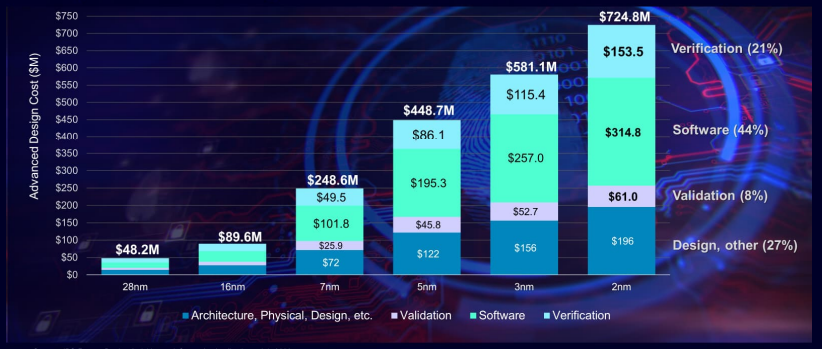
Software Key Component of Chip Architecture
- Increasing transistor count
- Rise in workload-optimized chips
- High mask and fab costs; first silicon success is crucial

Software Dominates Costs
- Software is a key differentiator
- Delays in software readiness are costly
- Essential for silicon sales

Chiplets and 3DIC
Moving monolithic SoCs to 3DIC and chiplet-based design



Design complexity driving cost!
Average cost for advanced design



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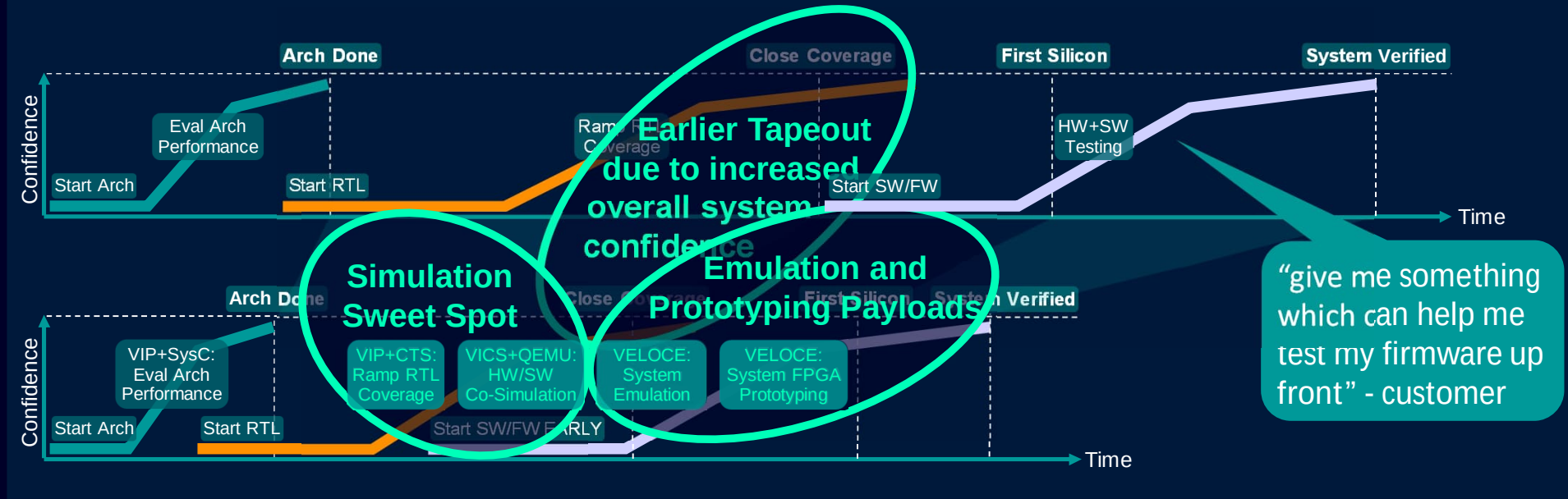
Accelerated Confidence from Siemens EDA – Software stimulus and early FW dev

Accelerated

Confidence

First To Market AND high quality via partnerships	Fast standard SV/UVM runs on all engines	Supports QEMU co-simulation for HW/SW co-dev	Sim Acceleration on emulator and prototype system	Tested on multiple controller designs from IP Partners	Finds bugs in design IPs that other VIPs miss	Future-proof Roadmap and Packaging	Broad Portfolio: Verification IPs + Compliance Tests

Virtual In-Circuit Simulation + QEMU – seamless shift from Sequences to Software, Accelerate HW/SW signoff



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Accelerated Confidence from Avery Verification IP

Accelerated

First To Market AND high quality via partnerships

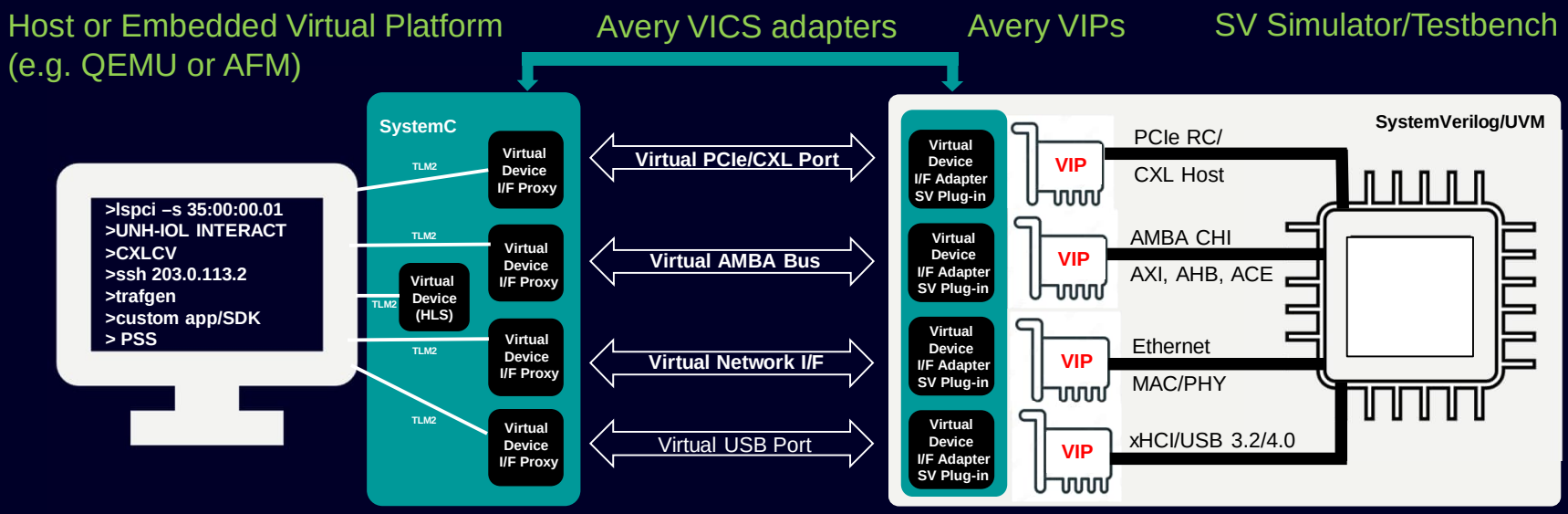
Fast standard SV/UVM runs on all engines

Supports QEMU co-simulation for HW/SW co-dev

Sim Acceleration on emulator and prototype system

Teste contr from

- QEMU and Arm Fast Models based Virtual Platform with TLM2 remote i/f
- Uses Avery SV/UVM VIP, remote Virtual Device I/F Proxies, VIP debug
- Supports hybrid virtual prototype modelling and HLS flows to RTL
- Multi-host and multi-embedded platform configurations
- No SV/UVM testbenches changes except adding VICS plug-in
- Enhanced HW-SW co-debug controls both SW and sim environments



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What EDA is doing to help? proFPGA prototyping plus Avery Speed Adapters

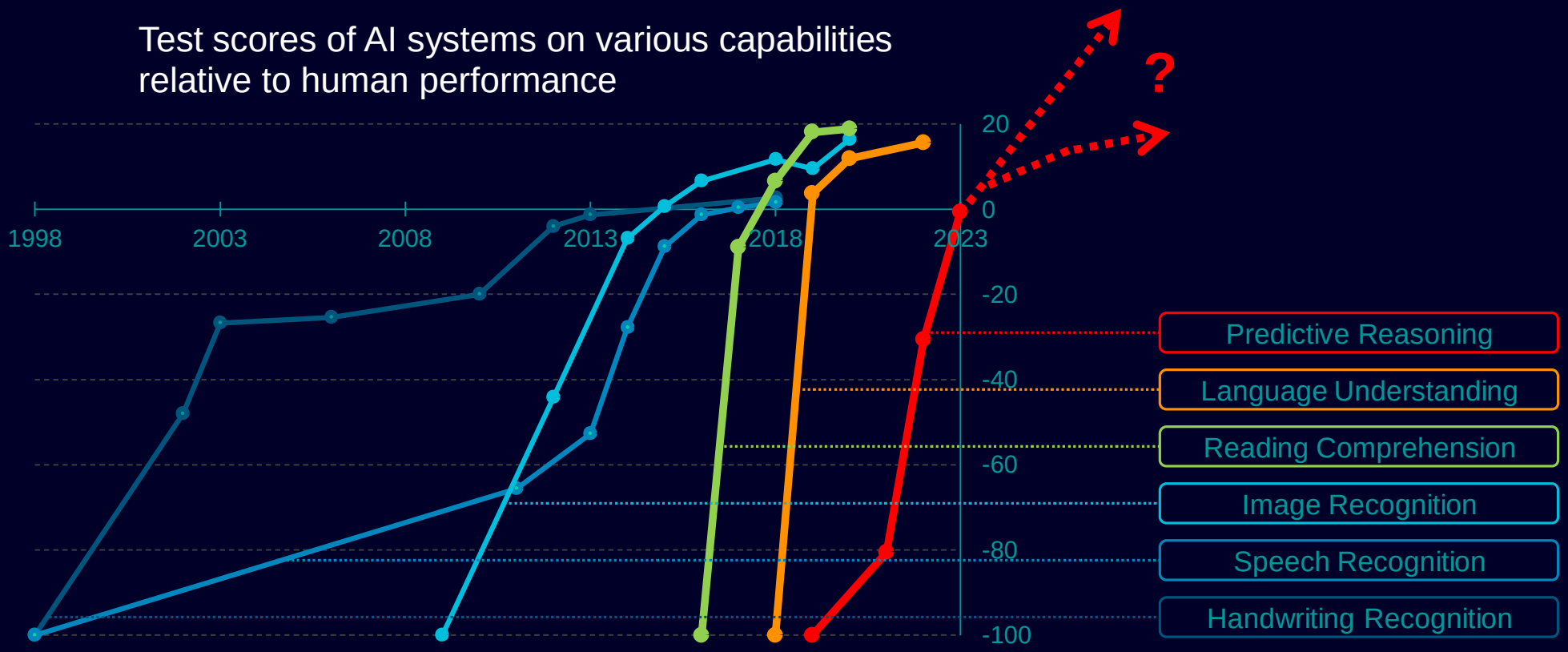
Advanced protocol Speed Adapters quality

- Veloce proFPGA is the prototyping reference platform for validation
  - Guarantees quality, performance and full compatibility
  - Easy access to proFPGA prototyping HW & SW platform
  - proFPGA modularity and flexibility allows to mimic customers' proFPGA setup
  - Large set of extension boards available with proFPGA
  - Automated, timing driven VPS user' software flow to synthesize and compile the design

Consolidated roadmap and vision for the future

- Timely availability of protocol speed adapters with proFPGA
- Alignment to customers' requirements: platform, extension boards and protocols

Huge AI chip design growth – Why now?



Data Source: Kiela et al. (2023) – with minor processing by Our World in Data

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What EDA is doing to help? Siemens Approach to Data and ML Innovation

Building on the strength of the larger Siemens organization

Collaboration

Partners

- Earlier Adopter Customers
- Access to Real Project Datasets
- Introducing Early Requirements

Siemens EDA

- IC and EDA Division Experts
- Open Source & Real Project Lifecycle Data
- AI and Data Science Central Group

Siemens Technology

- 1400+ AI Experts & 3700+ AI Patents
- Creating Verification Knowledge Graph
- Research on EDA AI Approaches

Data

EDA Expertise

AI Expertise

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What EDA is doing to help? Investing in future AI scale-up and scale-out Protocols

Some protocol examples:

NVIDIA NVLink and NVLink-C2C

NVIDIA solutions for scaling IO within server

- Enable high-speed, collective operations
- C2C Supports CHI and CXL layers
- Opportunity for custom VIP / partnership
- Opportunity for expert services business

Ultra Ethernet (UEC/UET)

Keeping up with throughput and latency needs of AI clusters

Ultra Ethernet Transport (UET) replaces RoCE, provides:

- Multipath, packet spraying, flexible delivery order, new congestion control, telemetry, efficient security built-in
- Larger scale, stability, and reliability

Infiniband

Legacy high performance network solution

- Competing with multi-GB ethernet
- Less well served with Verification IP
- Customer interest continues
- Need more industry / partner data

Ultra Accelerator Link (UALink)

Scale-up connect between AI accelerators and switches:

Open Industry Standard Interface for Enabling High-performance, Low-latency Communications Interconnect for Next-generation AI Accelerators in Data Centers

Newly forming consortium

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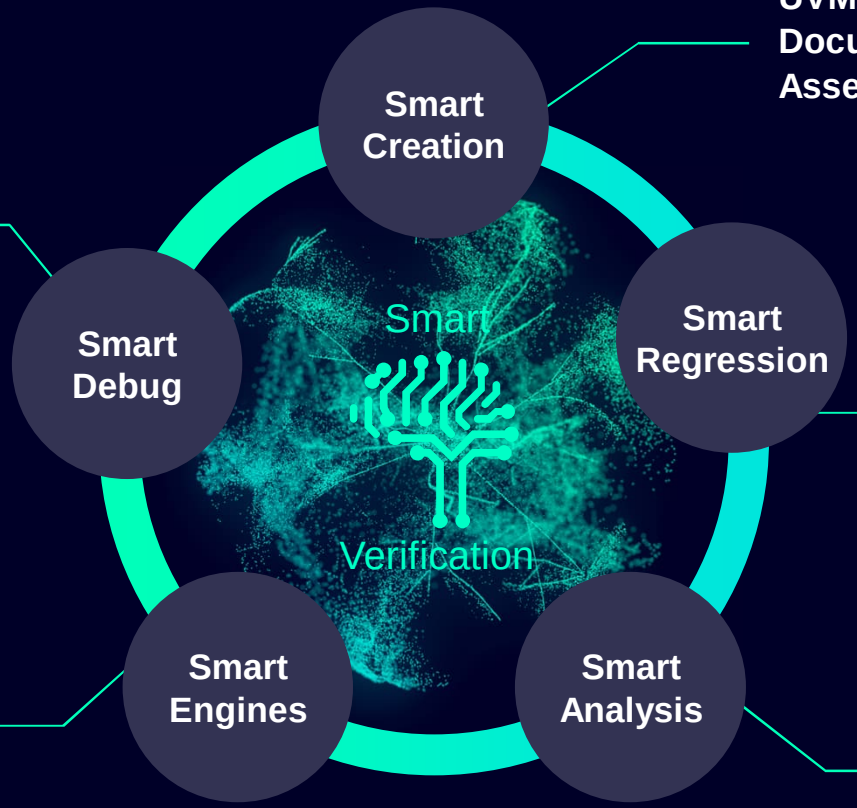
AI Maximising Verification Productivity

Faster Engines, Faster Engineers and Fewer Workloads



UVM and PSS Generation
Documentation Exploration
Assertion Generation

Failure Prediction
Smoke-test Prediction
Schedule Prediction

Pattern Analysis
Cross Hole Analysis
CDC/RDC Assist

Coverage Acceleration
Progressive Performance
Coverage Optimization

Bad Commit Prediction
Failure Signature Prediction
Root Cause Prediction

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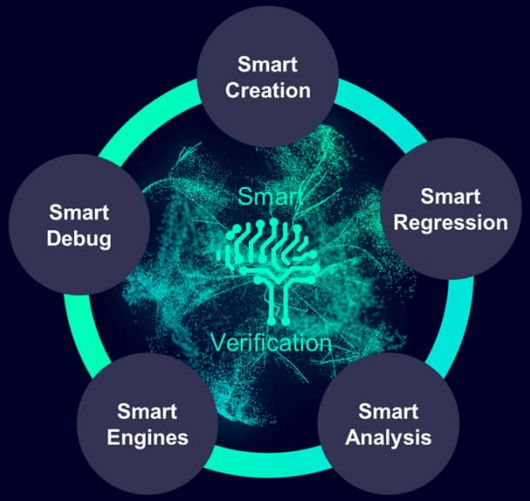
Questa AI Powered Smart Verification

Product	Technology	AI Value Observed
VIQ Coverage Analyzer	Pattern & Cross Hole Analysis	**3x** reduction in coverage closure time
CDC/RDC	CDC/RDC Assist	**90%** reduction in crossing violations
VIQ Regression IQ	Failure Prediction	**100x** faster to find first failure and **2x** faster to find last failure
	Smoke Test Prediction	**10x** reduction in smoke test regression time
VIQ Debug IQ	Bad Commit Prediction	**2x** reduction to find and confirm bad check-ins
	Signature Prediction	**30%** reduction in overall debug time
Questa Sim	Coverage Acceleration	**100x** faster time to coverage closure with **500x** fewer tests



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Summary
Harnessing Collective Wisdom Across Tools, Processes, and People

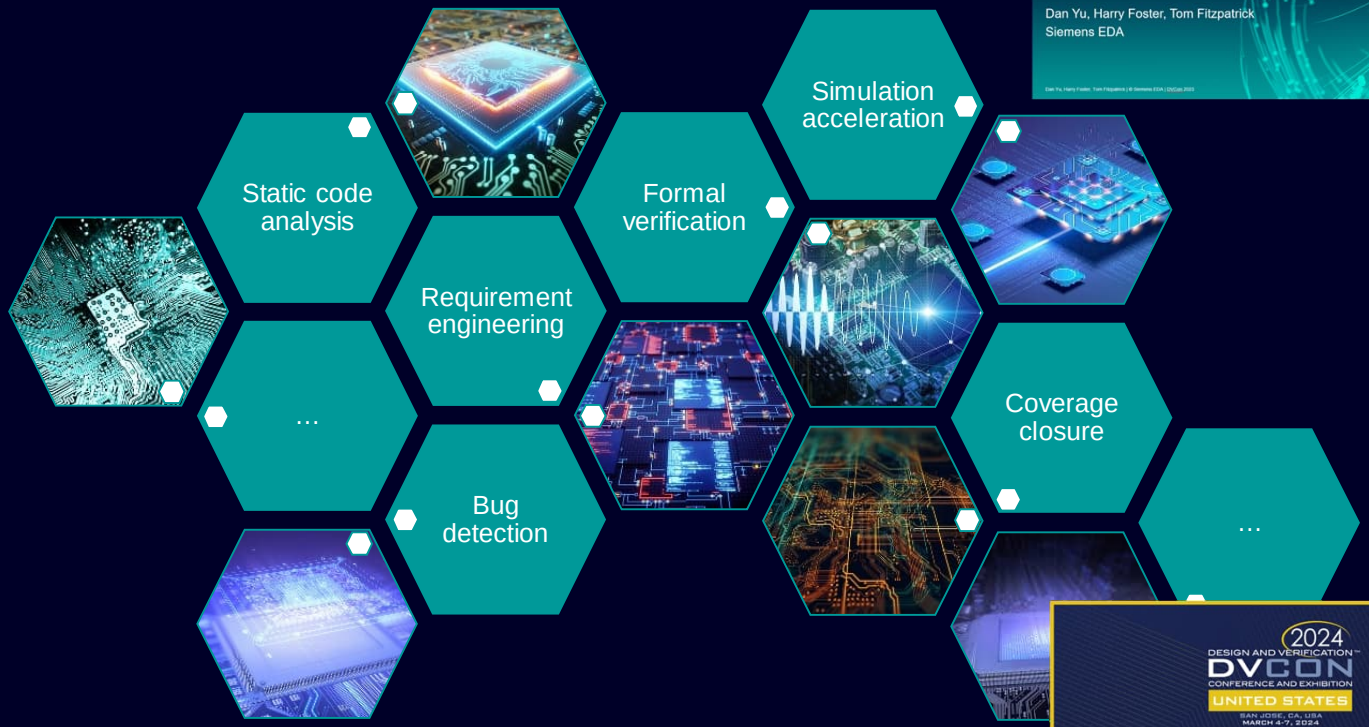
AI is a means to achieve transformation, not an end in itself
- Natural language is not suitable for complex design description
- Generative model need to be enhanced to handle long sequences and relationship of those tokens
- Specific agents should be built to have domain specific knowledges

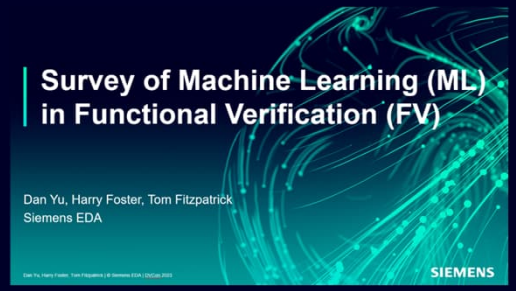
Macro Trends
- Semiconductor transformation
- Data explosion changing everything
- Movement to Software Defined Products
- Decline in engineering talent demands smarter verification
- Sustainable solutions is no longer an option

The need for Accelerated Confidence
- Complex 3DIC verification, enabling Software co-simulation, effective prototyping acceleration

Verification is Fundamentally a Data Problem

A survey of published research





DVCon US 2023 Paper

DVCon US 2024 Paper

Source: D. Yu, H. Foster, T. Fitzpatrick, "A survey of machine learning applications in functional verification," DVCon US 2

Source: D. Yu, et al., "Large Language Model for Verification: A Review and Its Application in Data Augmentation" DVCon

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