2024 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION TAIWAN

The ASIC Renaissance

A Glance into the Future SoC Enablement

By

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accellera SYSTEMS INITIATIVE

Who Are TESDA?

- An innovative startup focused on SoC DV & architecture optimization automation. With such innovations, we hope to renovate the world to become a better place.
- Board of Directors and Advisory Committee

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Board Member and CEO

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A Question for the Audience

- Over the past several decades, silicon technology has profoundly transformed and elevated the quality of human life. As we look to the future, what hardware innovations will continue to drive this remarkable progress in the next three decades?

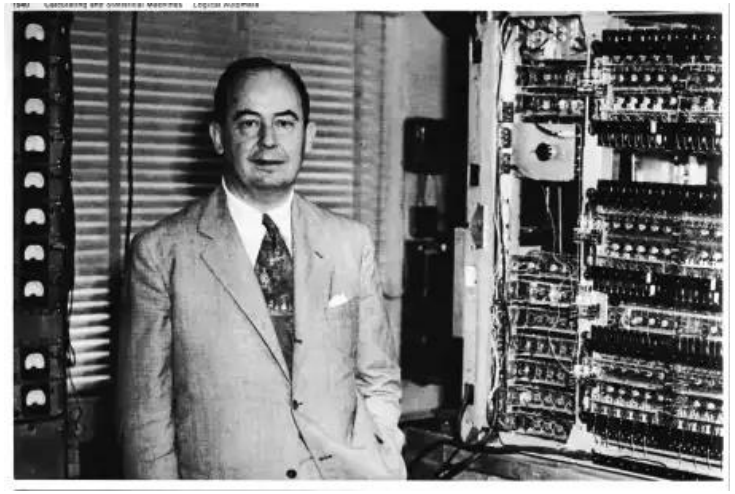
a) Quantum technology

b) New material systems like Carbon nanotube, 2D material, protein etc.

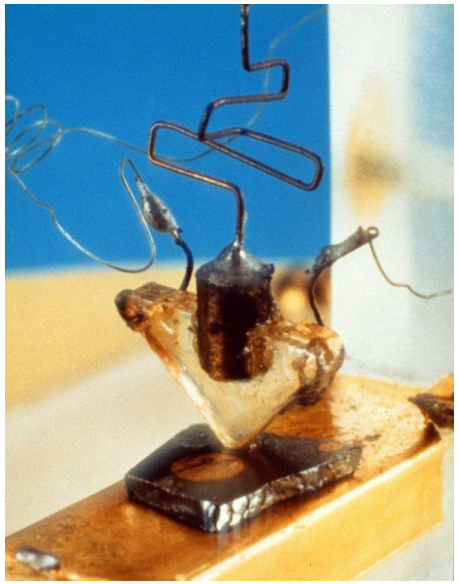
c) Same old silicon technology

My Belief Is

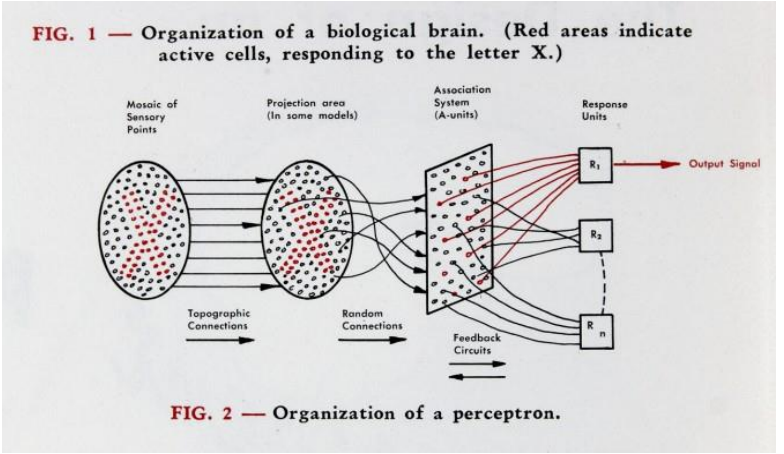
- The same old silicon technology.
  - Any technology will need at least 30 years to mature to have major impact. If they are not available now, will not have significant impact for the next 30 years



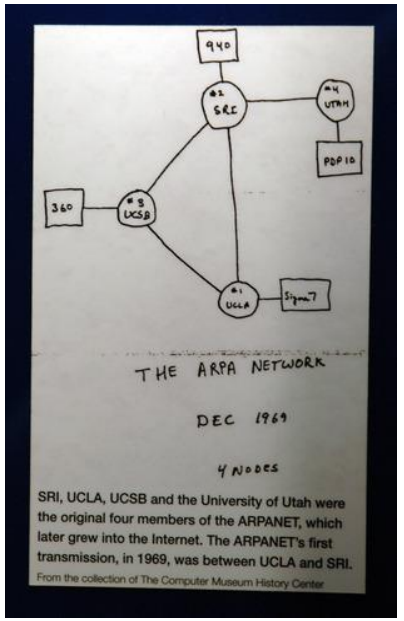
Modern computer from 1945



Transistor from 1947



Neural Network from 1958



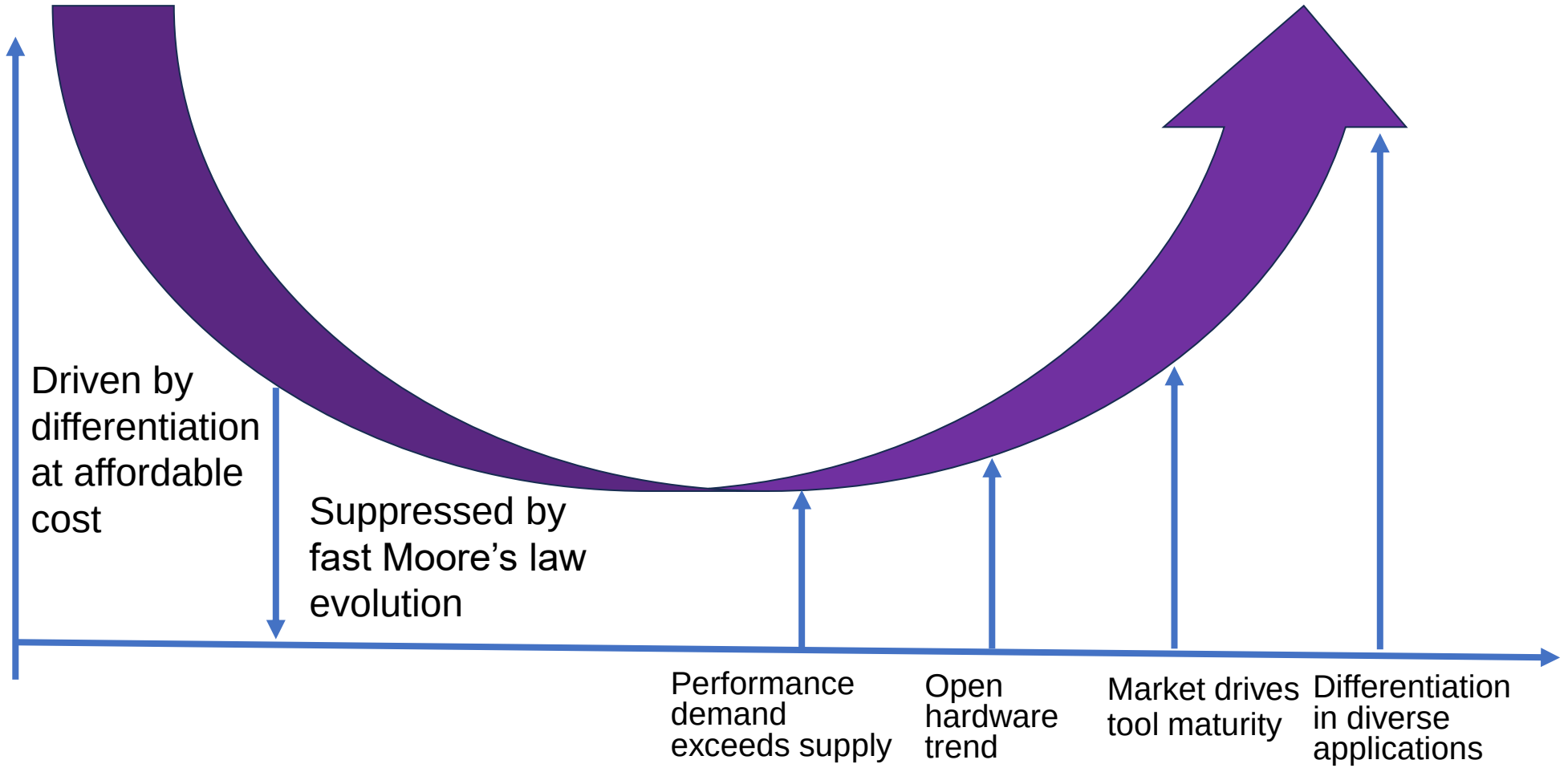
Internet from 1969

What Is the Implication Then?

- How to renovate the silicon technology for the next 30 years with affordability, just like last 30 years?

- It will be ASIC!
  - Creating value not just from Moore's law
  - It is not new, but new methodology is needed to make it available for the mass.
  - From innovate to renovate.

ASIC Adoption Curve



Main Challenges for Custom ASIC Development

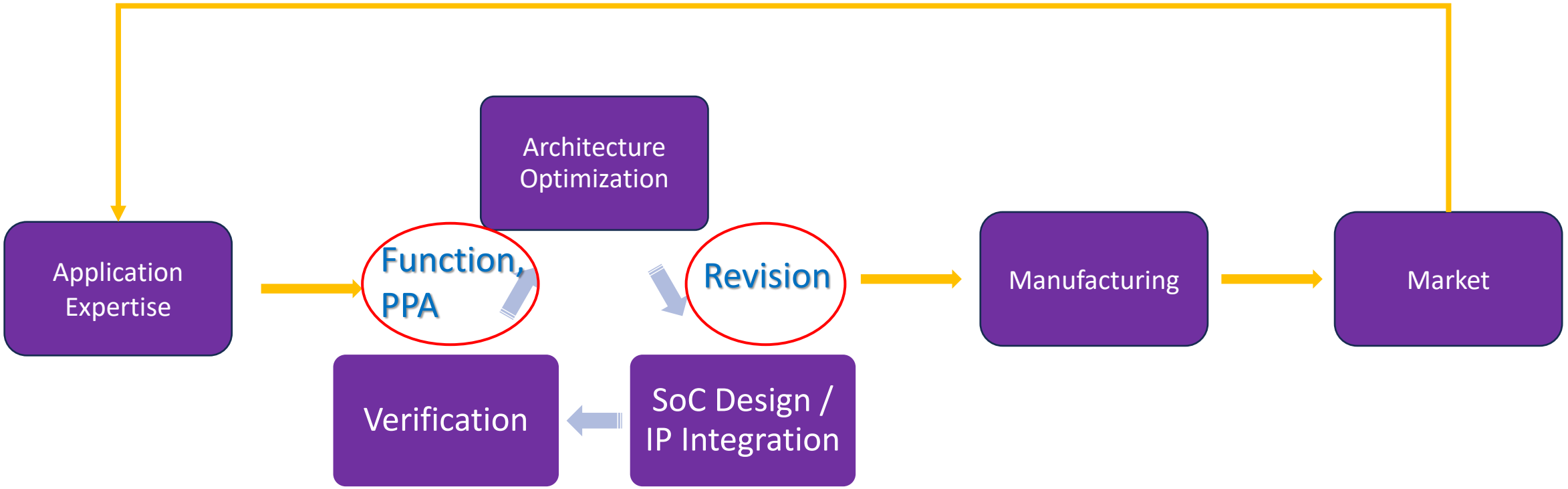
Can we share the cost and resource?

Will early virtual prototype, ecosystem and LLM help?

Some redundancy for trade-off?

NRE	• A risk factor • Barrier for smaller companies
Time to Market	• Another risk factor • Design/verification is the major portion
Knowledge	• System/application to IC language difficult • Vertical market knowledge are diverse
Design & Verification	• Verification complexity scales faster than design • Optimal architecture at early stage is a question
Flexibility	• Difficult to change in comparison with suboptimal FPGA or off-the-shelf components

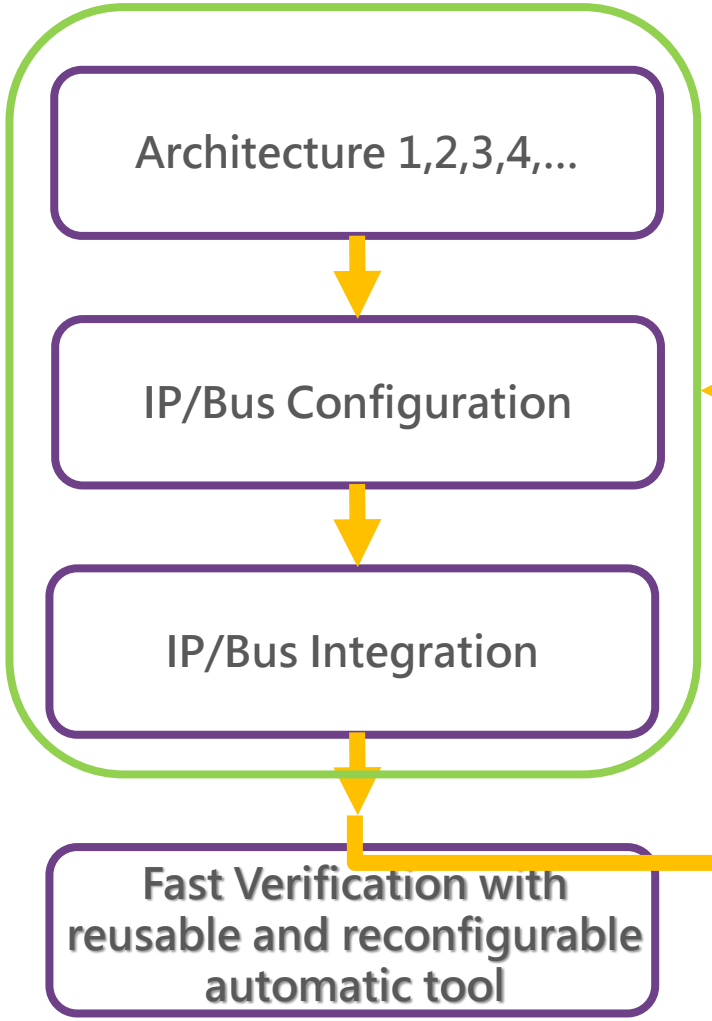
How to Make a Great ASIC?



- How do you know the revised architecture is better? What are the trade-offs?
- How do you modify and get the verification results quickly?

Fast Verification Can Change Everything!

Other than top-down ESL methodology driving from algorithm and down, we complement with a bottom-up one.



Fast iteration towards convergence of desired architecture

Raising Verification Abstraction Level

High

Tools

Abstraction Level

Level 3: SoC Level

Verify mutual interference from concurrency between subsystems

Level 2: Subsystem Level

Verify the interaction between IP/Blocks

UVM and VIP

Level 1: IP/Block Level

Verify the integrity of each IP/Block

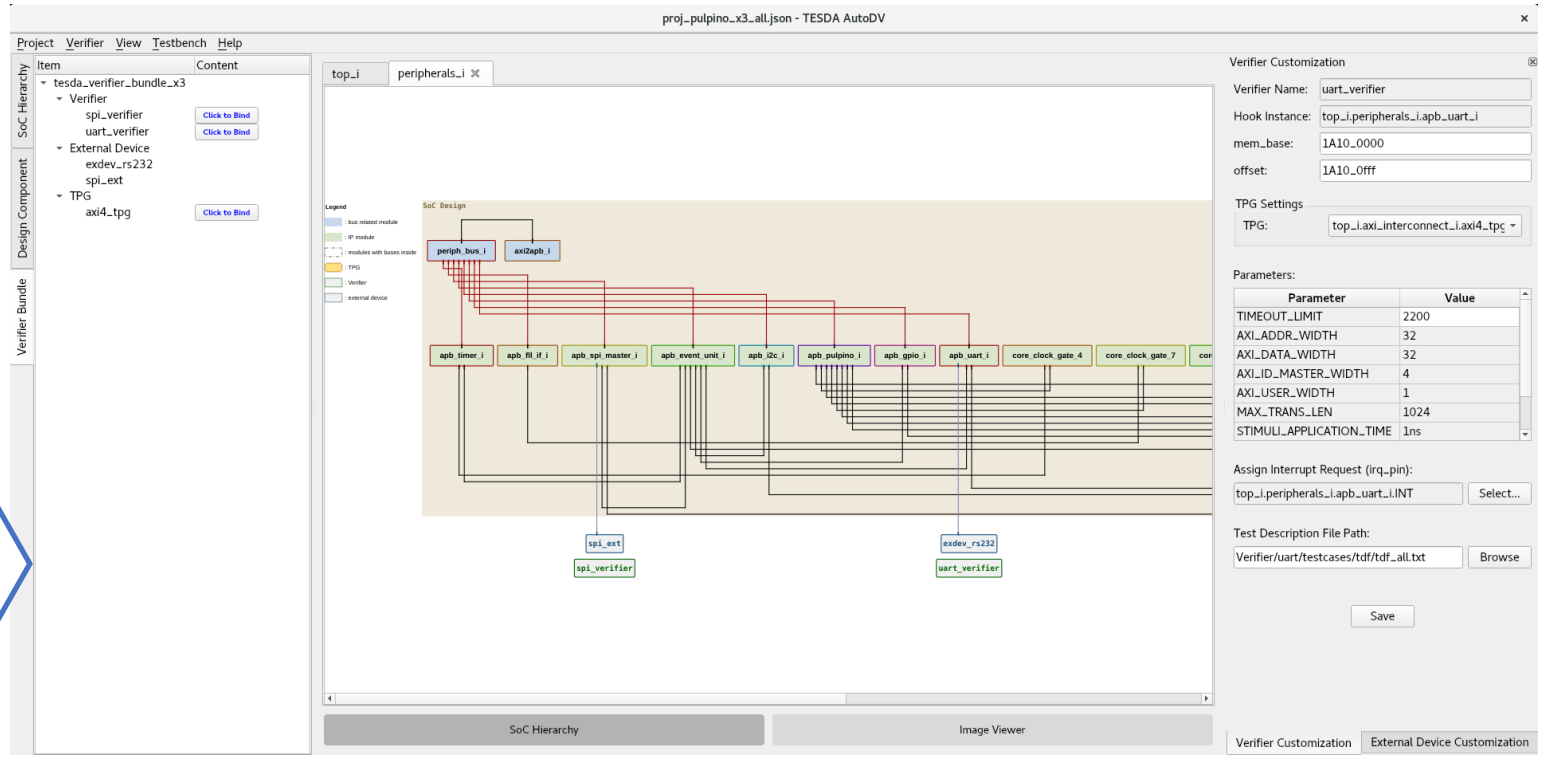
Low

TESDA AutoDV® as an Example

Automatic tool raising verification abstraction level from IP to subsystem

SoC Design

Auto-fusion, configurable sub-system test suite library



Ready for Simulation Test Bench

Conclusion

- ASIC will be the foundation technology driving the welfare of human life for the next several decades.
- How to overcome the design and verification challenges and be available to different vertical markets?
  - Innovative automatic architecture optimization and verification tool
  - Ecosystem support
  - Platform based offering
  - AI enablement
- It is not possible to predict the future, but we can shape the look of future through our collective effort.