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2024 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION TAIWAN

2024 RISC-V Taipei Day

AutoDV: Boost SoC Verification by Automatic Environment Construction

Robert / Chi-Kang Chen
CEO@TESDA, Sep. 11, 2024

Who Are TESDA

- An innovative startup focused on SoC DV automation.
- Board of Directors and Advisory Committees

Dr. Kurt Huang
Chairman

Robert Chen
Board Member and CEO

David Wang
Board Member and Adviser
Senior VP, GPU Technologies and Engineering

Prof. Shi-Yu Huang
Research Adviser
Director General, STPI, NAR Labs

Terry Tsao
Marketing Adviser
Global CMO & President of Taiwan, SEMI

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Where Are TESDA

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SoC DV Automation

- Block Verification
- Simulator
- Emulator
- FPGA Prototyping
- Synthesizer
- Place and Route
- SPICE and Timing Analysis
- DFT and Physical Verification
- Emerging Issues
  3D Stacking / Chiplet / Advanced Process and Packaging

SYNOPSYS®

cadence®

SIEMENS

Incubation Center@ITRI
3rd to 5th floor, Building 53

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SoC Verification Challenges

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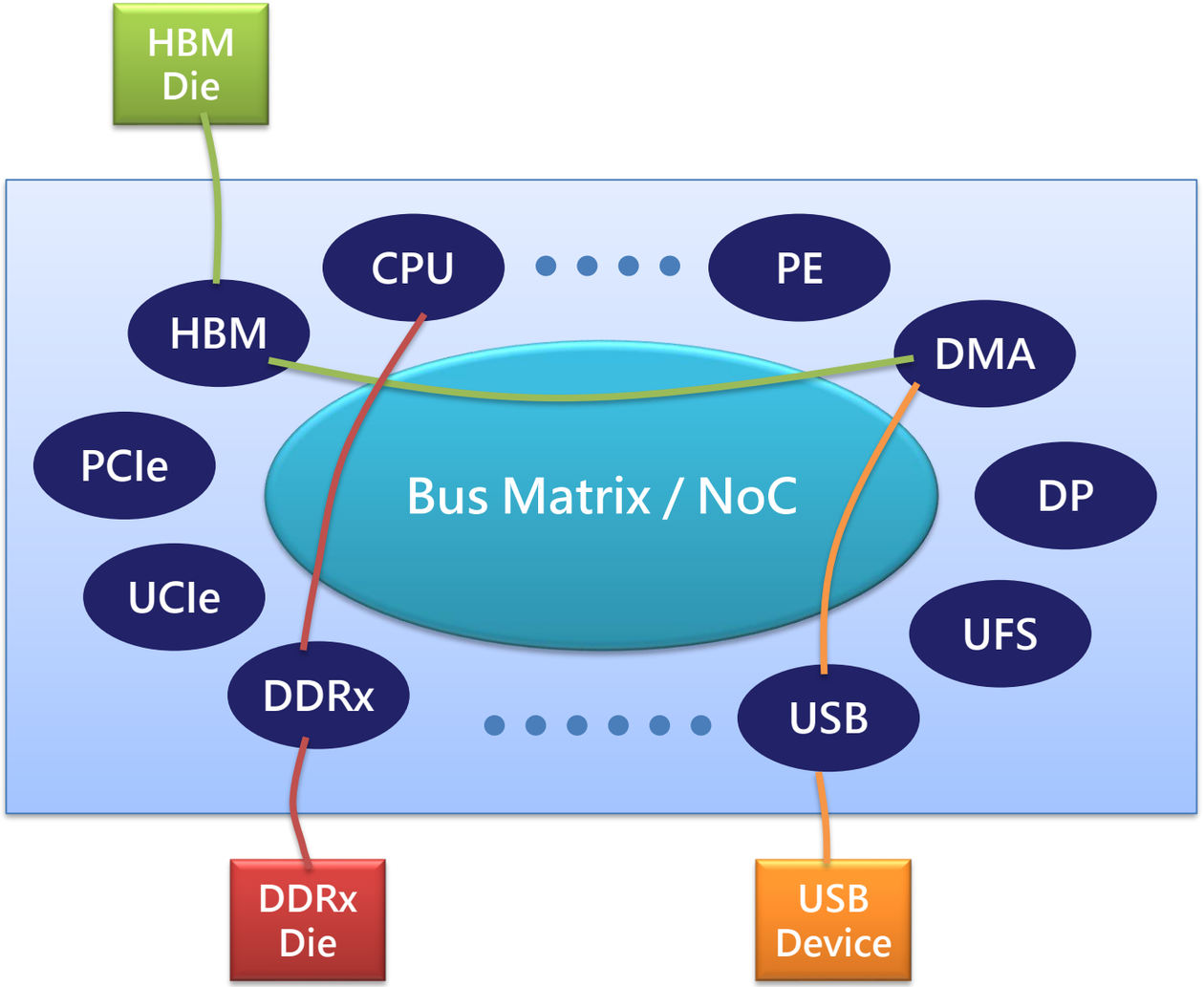


Quantity issue:

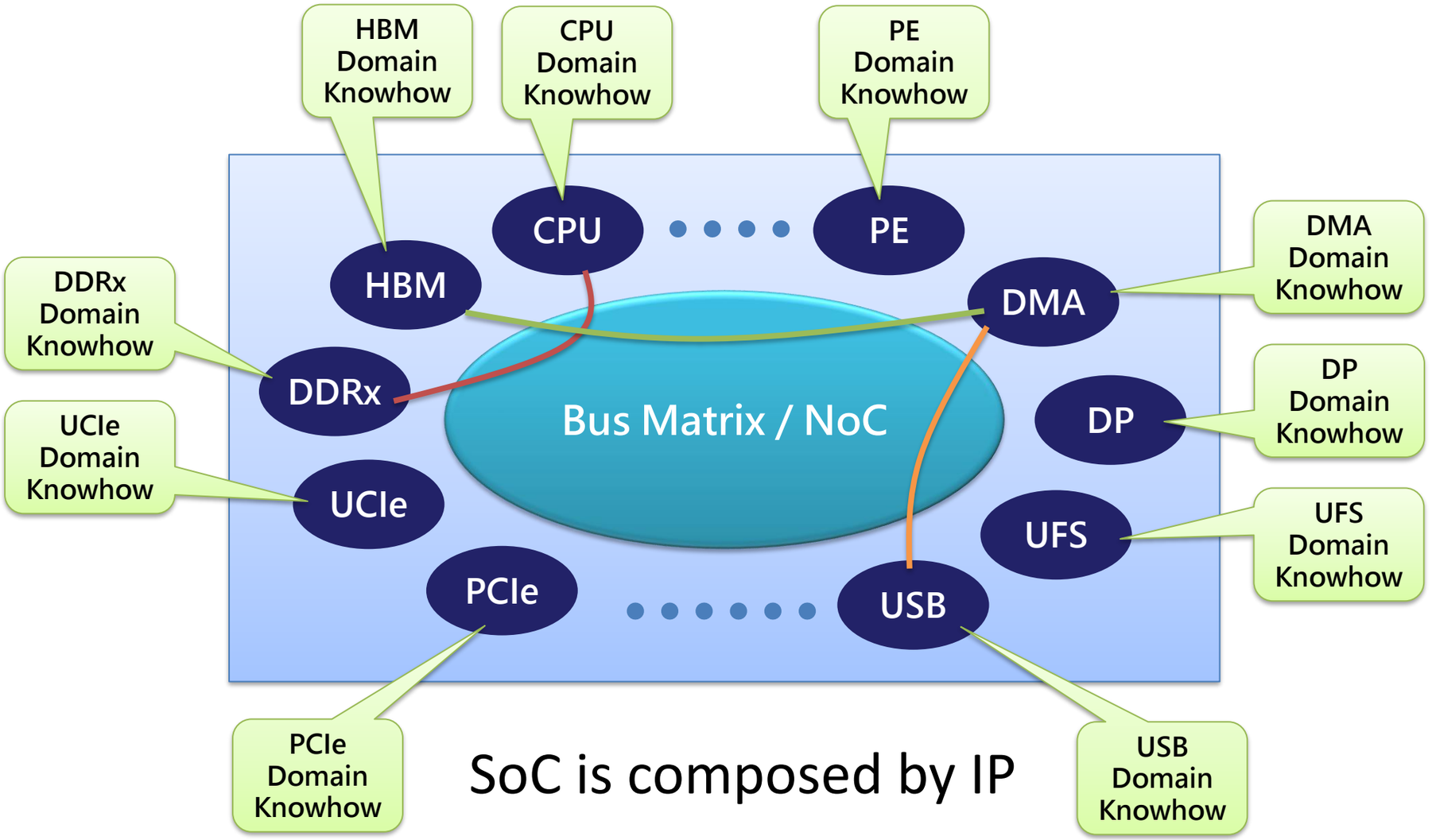
- So many possible Subsystem
- So many possible Concurrency

S

M

	IP 1	IP 2	…	IP N
IP 1	X	O		O
IP 2	O	O		O
…				
IP N	O	X		X

SoC Verification Challenges



SoC is composed by IP

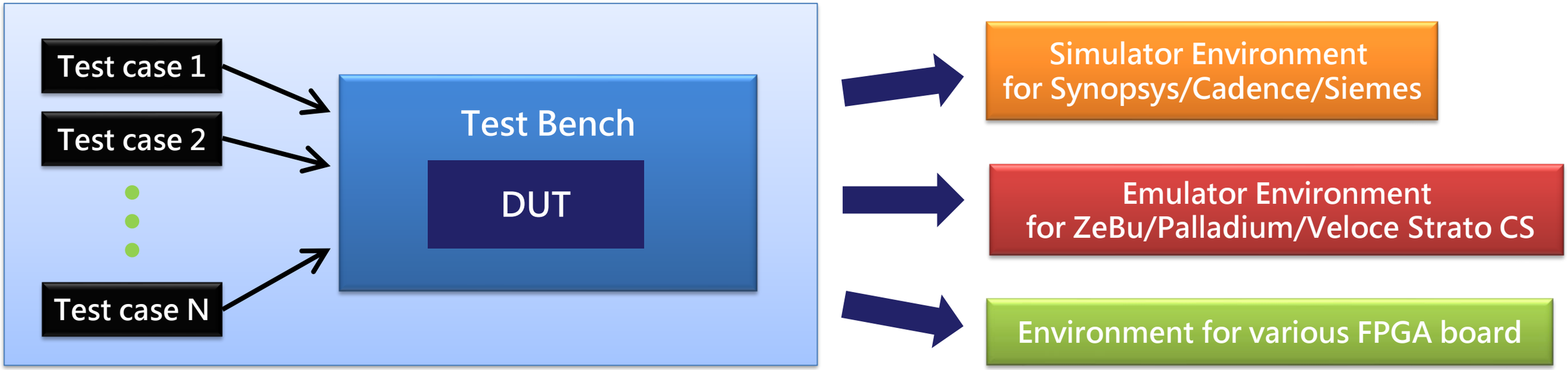
Quality Issue:

- So many Domain Knowhow required
- So many IP/Bus/NoC configuration possibility

SoC Verification Challenges

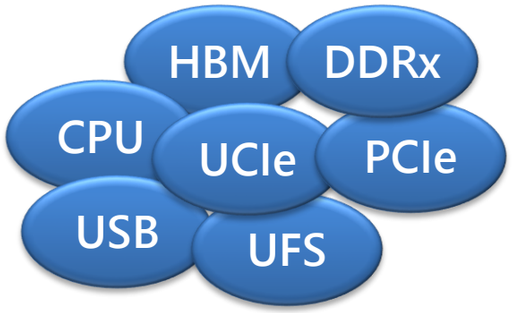
For each Test Bench and corresponding Testcases…

Environment Issue:
- So many different simulator
- So many different emulator
- So many different FPGA

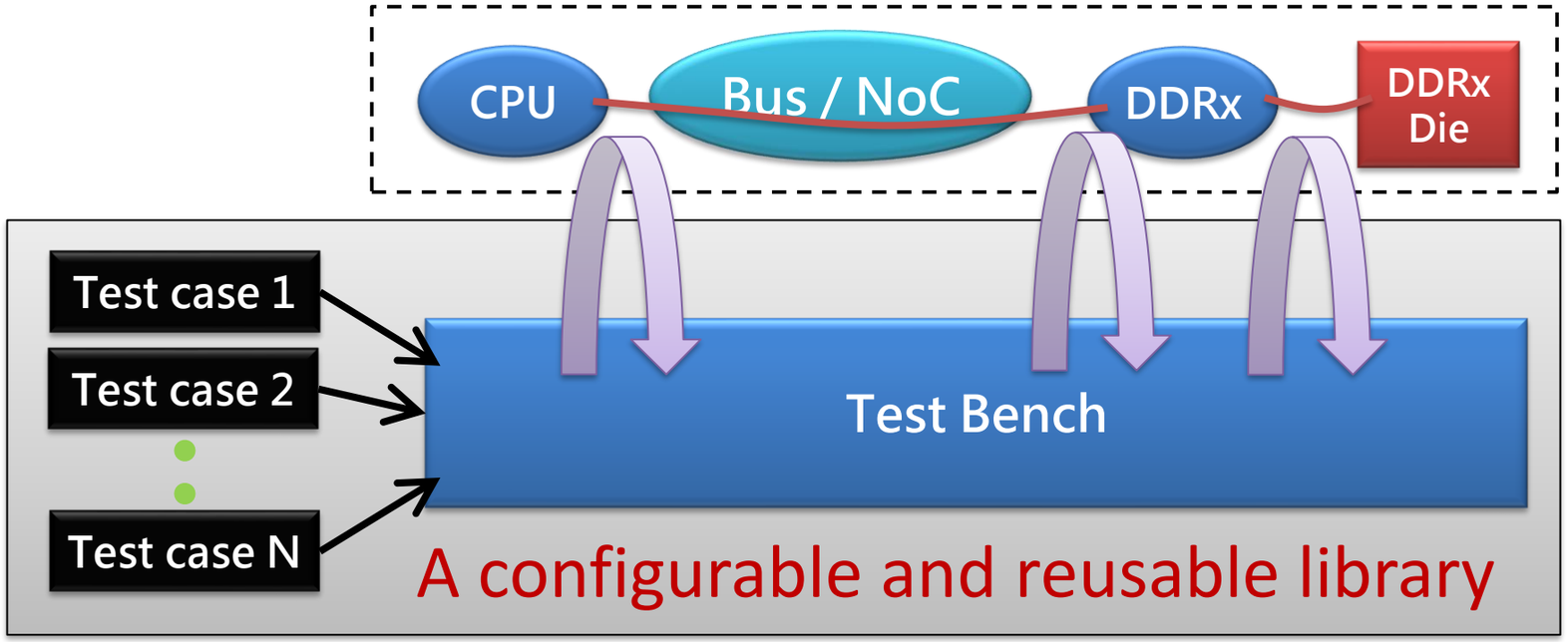


Observations

Many silicon IPs are commodity/reused.



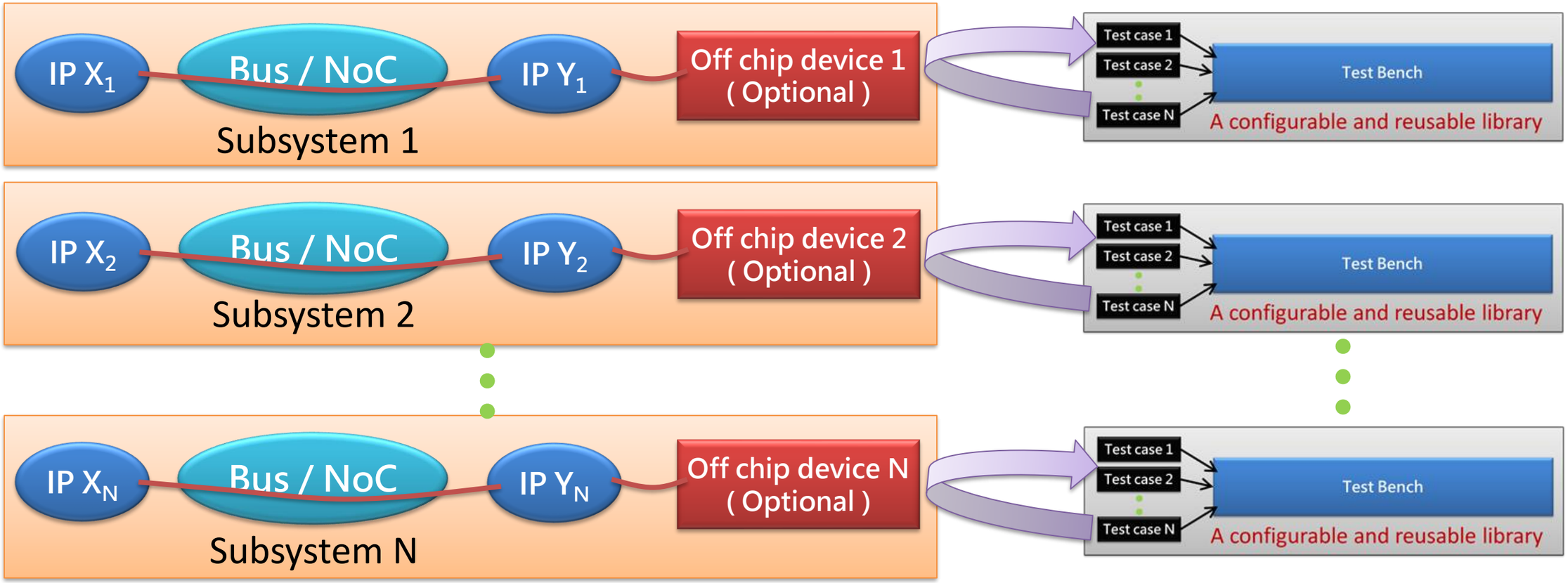
Subsystem composed by silicon IPs is a fixed signal link



Key Idea

Elaborate every subsystems within a SoC

Build TB and TC for Construct



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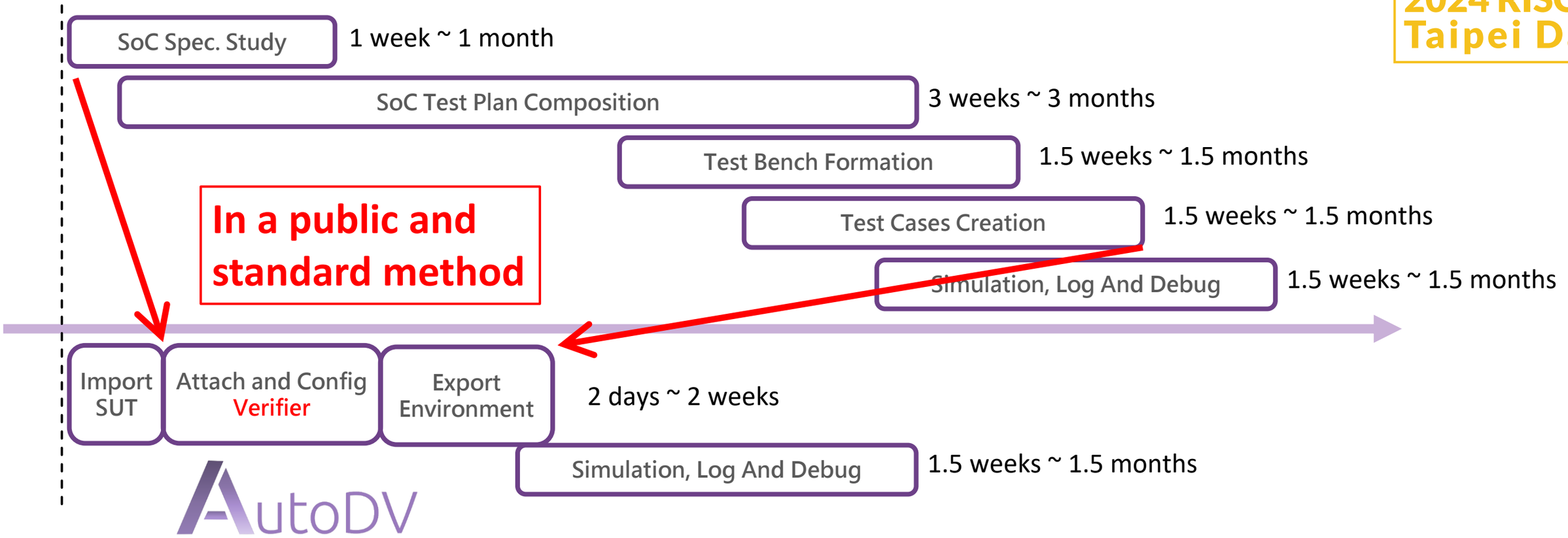
Knowledge Encapsulation



- **Encapsulate and reuse knowledge via proprietary Verifier library**

Before: 7 weeks ~ 7 months

Before: 80~120 man-month

After: 2 days ~ 2 weeks

After: 8~12 man-months

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Boosting Verification Efficiency

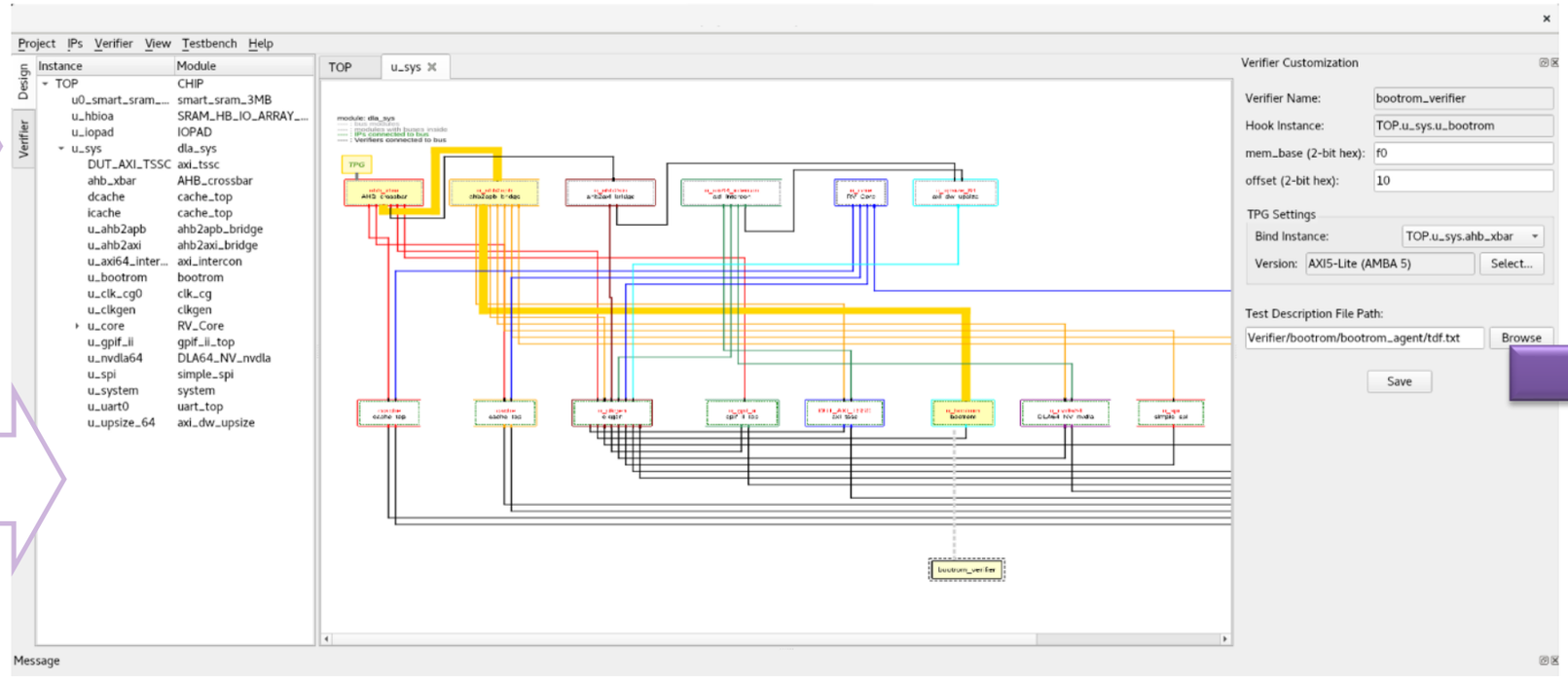
AutoDV

1. Import

SoC Design

Verifier (Configurable Sub-system Testbench)

2. Attach and Config



3. Export

Ready for Simulation/ Emulation/ FPGA Environment

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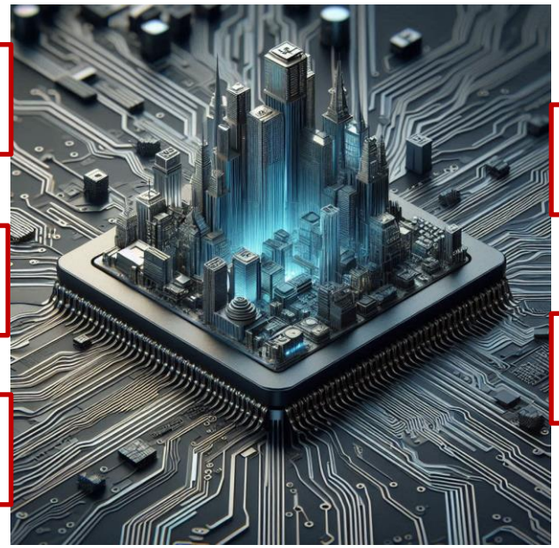
WHY WE DO ALL THIS

- SoC is getting more and more complex

Quantity issue

Quality issue

Environment issue



Lack of DV Engineer

Very Tight Schedule

Construct Automation →

Knowledge Encapsulation →

AutoDV

← Public and Standardization

← Highly Reusability

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Welcome to our Booth

THANK YOU