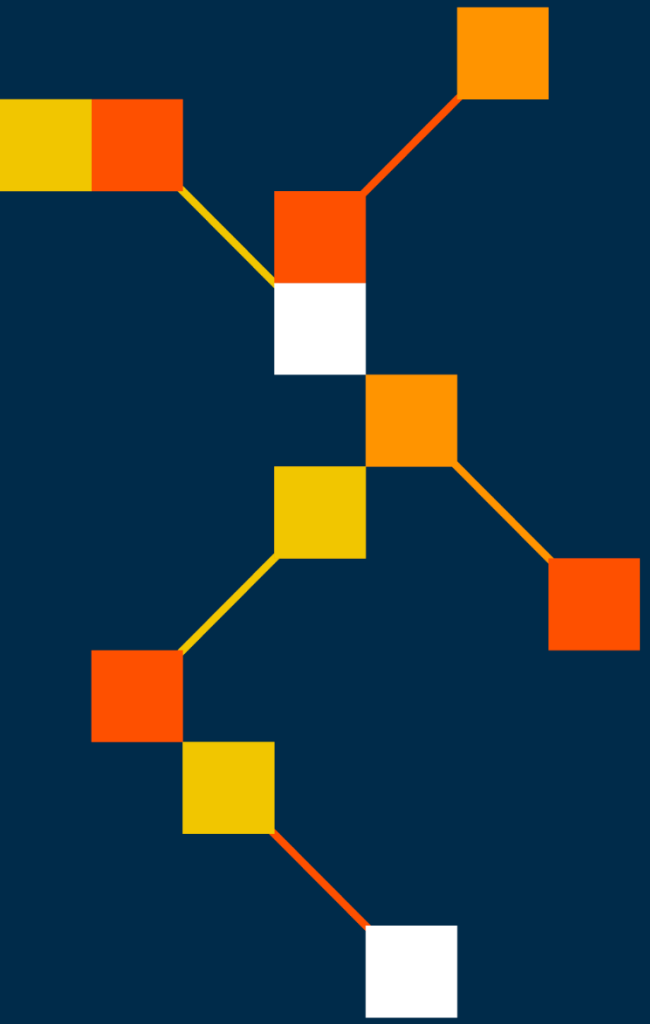


Boost SoC Development Efficiency with Arteris SoC Integration Automation Solution

Automate Design Flow and Register Management

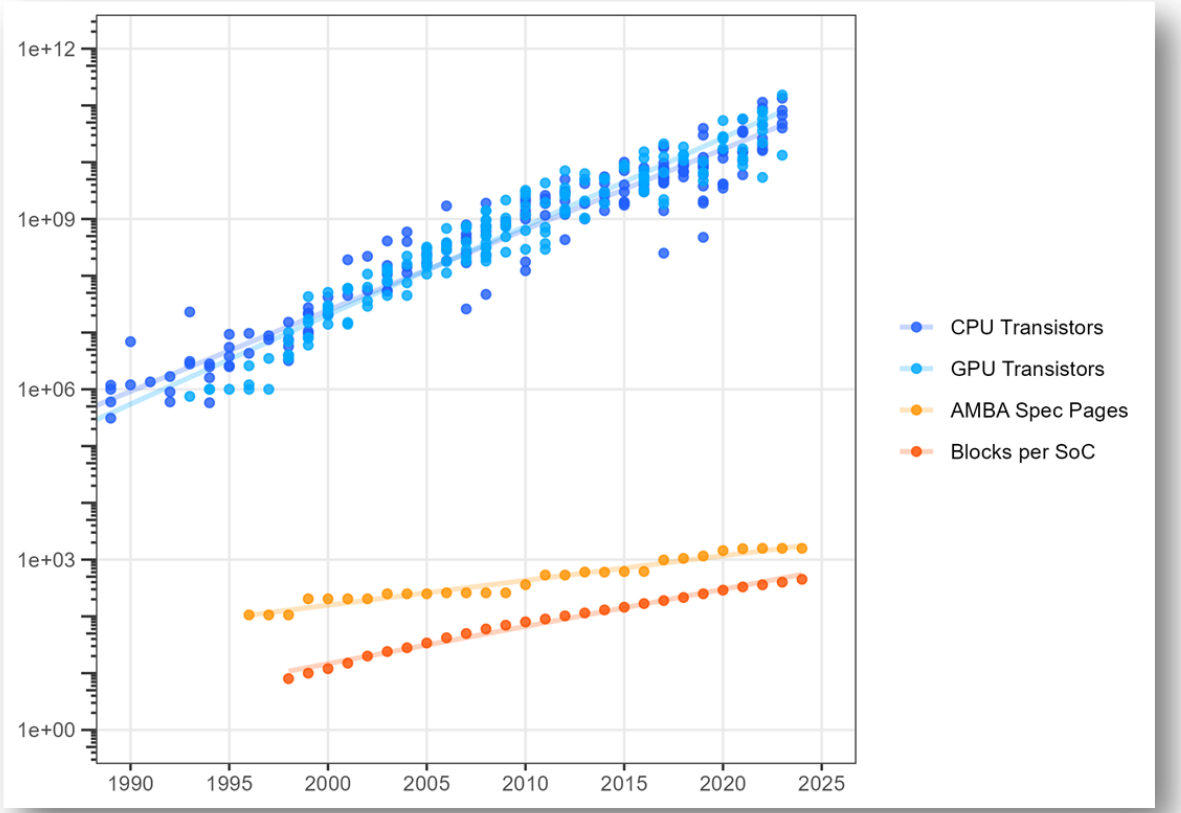
YiChiang Chang
Senior Field Application Engineer

September 11th, 2024

ARTERIS IP

Industry Challenges

- Designs continue to grow in size and complexity
  - 500+ up to 1K IP blocks
  - 200K+ up to 5M+ registers
- HW/SW Interfaces (HSIs) are critical
  - Many disciplines involved in the development process
- Limited cross-team synergy
  - Despite the need to collaborate effectively
  - Team “silo’s” and serial design process
- Miscommunication
  - Lead to specification misalignment
  - Can cause disaster and may require late fixes or even re-spins if issues cannot be resolved in software
- Inconsistent data (HW/SW/documentation) across proprietary or legacy databases and flows
- Many different forms of definition exist - Spreadsheets, IP-XACT, SystemRDL…

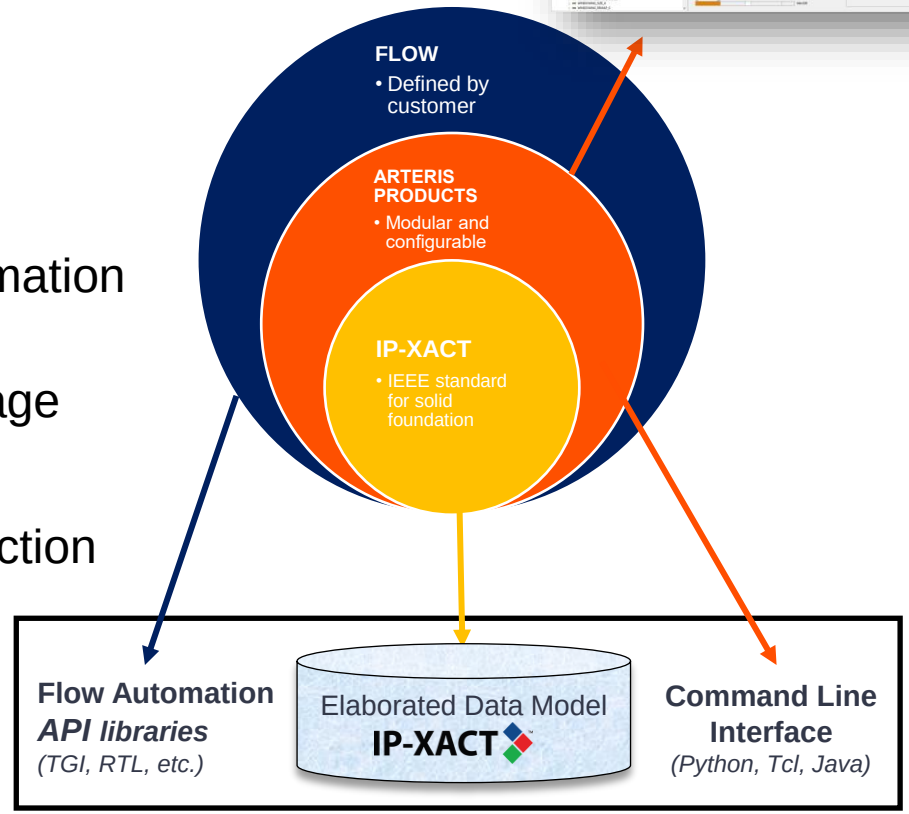


Source: Arteris, based on https://rb.gy/qmfcn, https://rb.gy/pgdop, The SHD Group, public protocol specs

Addressing the industry challenges

Embracing the IP-XACT standard

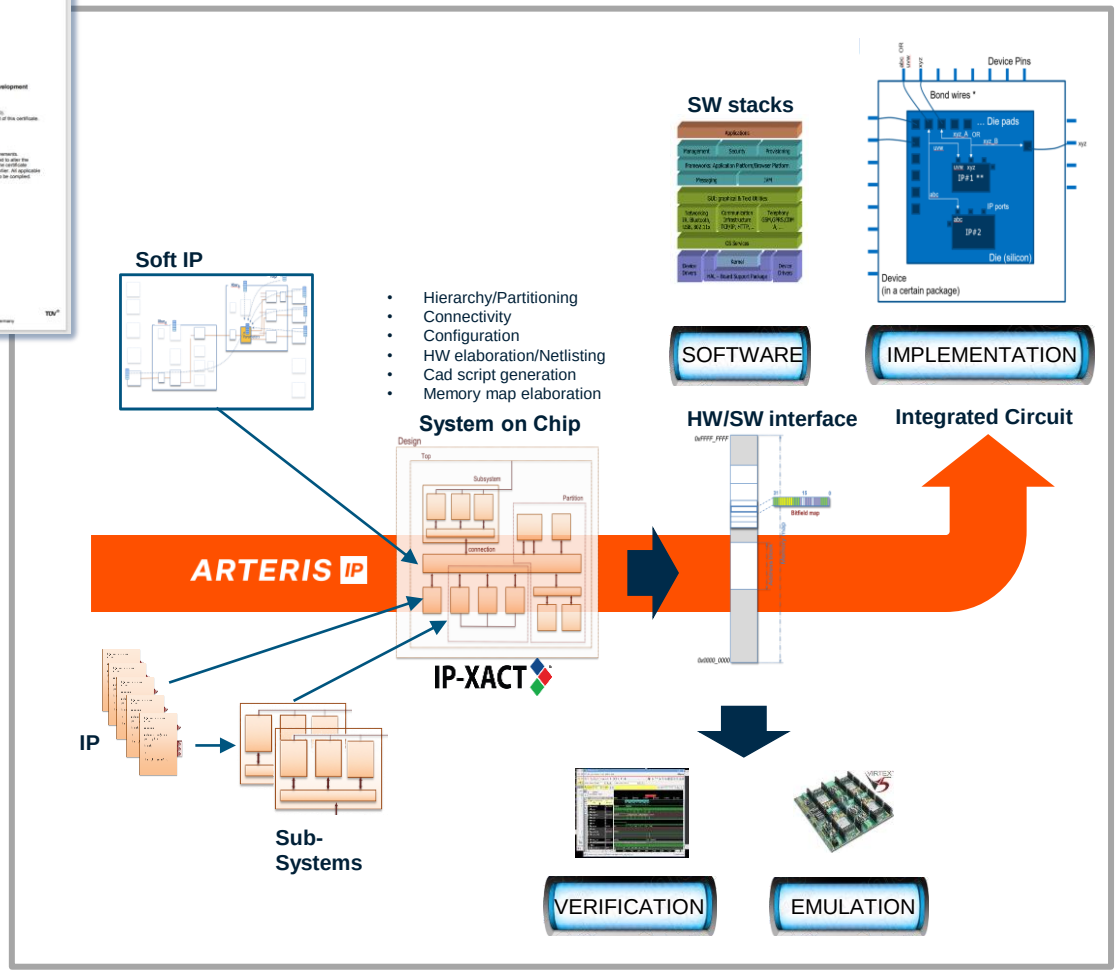
- IP-XACT: IEEE 1685 standard
  - http://accellera.org/activities/working-groups/ip-xact
- What IP-XACT enables:
  - IP re-use with a universal format to exchange and reuse information about IP and subsystem
  - Higher level of abstraction compared to traditional HDL language
  - Internal team cooperation ensuring data consistency
  - Built in checkers for better quality design with early issue detection
  - Enable efficient automation thanks to XML
  - Facilitate interoperability
- Mature and widely adopted
  - IP provider and EDA tools vendor supports IP-XACT
  - Customer and purchaser request IP-XACT delivery



Introducing Magillem for SoC Integration Automation

- ISO 26262-TCL1 certification
- IP and design reuse
  - Best-In-Class IP-XACT packaging
- SoC integration / Platform assembly
  - Rule-based connectivity – feedthrough
  - Table-based assembly flow
  - Collaborative work with IP updates, diff and merge capabilities
  - RTL restructuring / Hierarchy manipulation / Design derivatives
  - Generation of top-level netlist and makefile scripts for EDA tools
- HW / SW interface – Register management
  - UVM, Register bank, C header, Docx, html, etc.
  - System map
  - FuSa Reg bank
- Design Flow automation – CAD flow
  - Batch mode execution

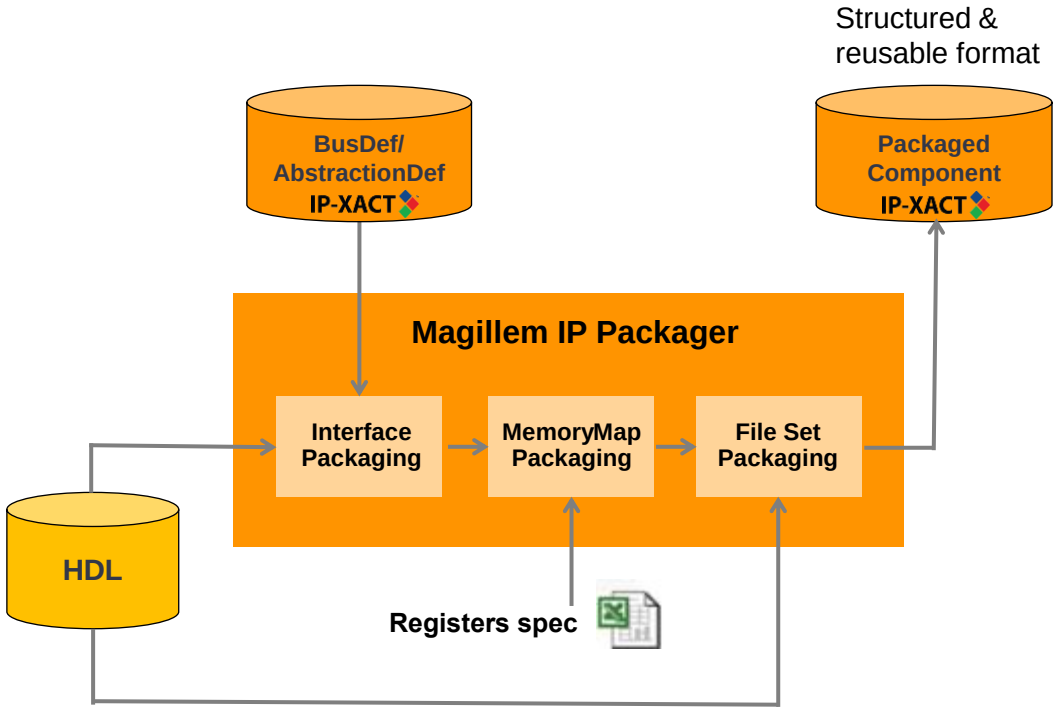

CERTIFICATE



ARTERIS IP

IP Packaging & Assembly Flow

Facilitate IP reuse and SoC integration



Automated data extraction from different sources

Project Settings
- Workspace and directory's structure
- Import catalog
- Set preferences

Assembly
- Instantiate components
- Create connections
- Configure your design

Virtual hierarchy (optional)
- Define virtual hierarchy
- Move, merge, or flatten
- Generate new hierarchical project with component based on new hierarchy

Netlister
- Run checkers
- Generate VHDL, Verilog or SystemVerilog netlist

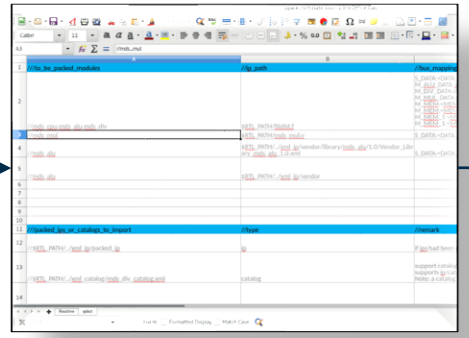
Makefiles
- Generate makefiles EDA tools:
  - simulation: Cadence, Mentor graphics
  - synthesis: Synopsys
  - Prototyping and emulation: Synopsys, Xilinx, Cadence

Sanity checks
- Compilation and elaboration
- Synthesis: techno target and prototyping platform
- Linter and CDC checks

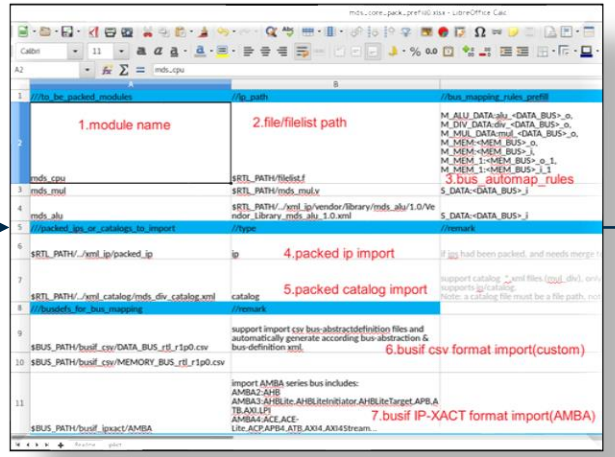
ARTERIS IP

Table-based Assembly Flow

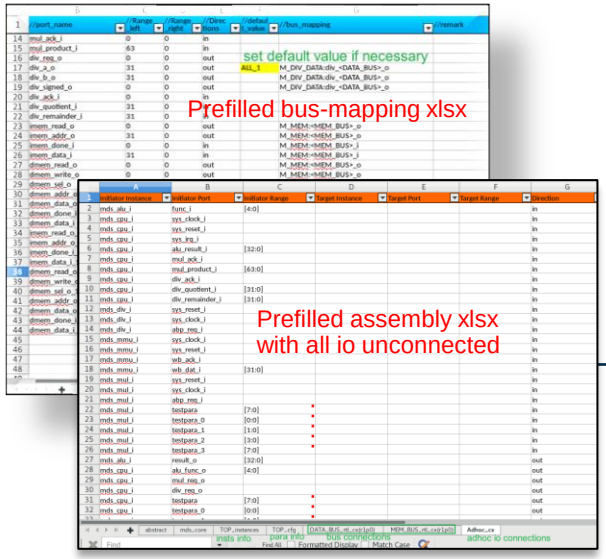
cmd: setup



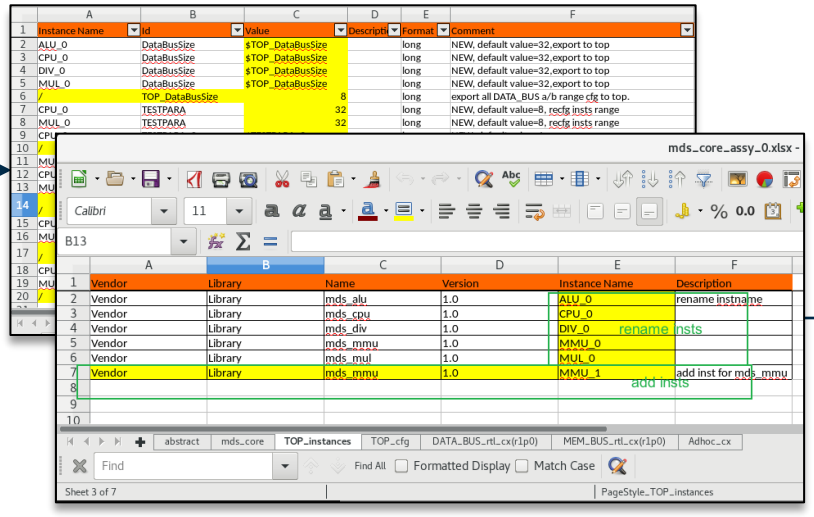
Get an empty xlsx template



Fill ips/busifs/xmls/bus_mapping rules in the iplist sheet

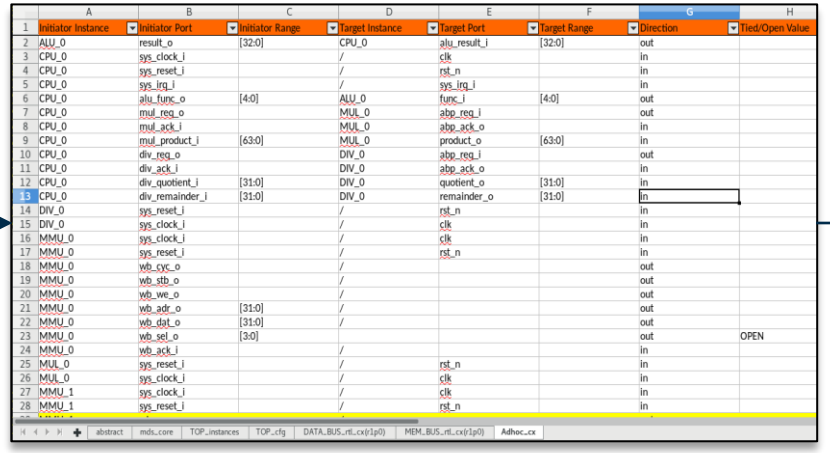


Get a bus-automapping prefilled table & initial assembly xlsx



Rename/add/delete insts/export or re_cfg parameter in TOP_instances/cfg sheet.

cmd: update



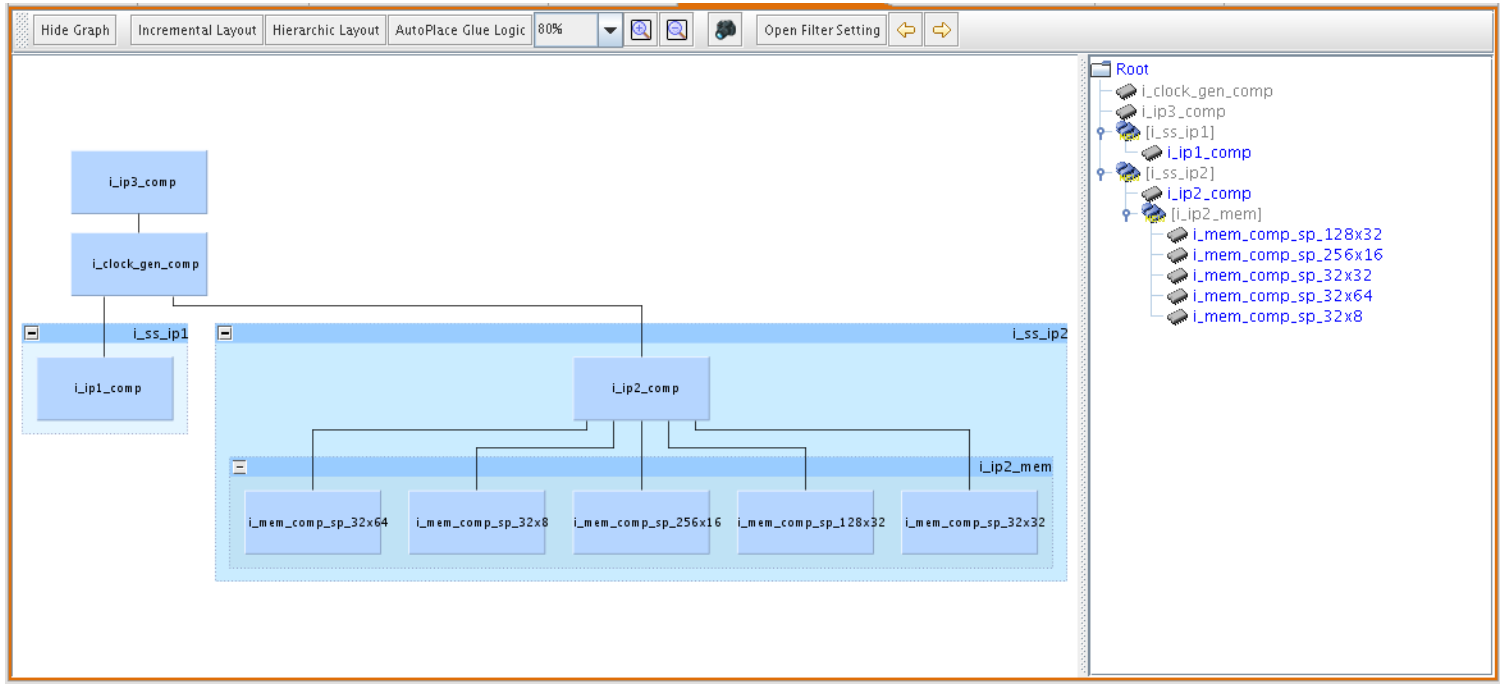
Do bus_cx or adhoc_cx connections based on newest IO range

cmd: tba

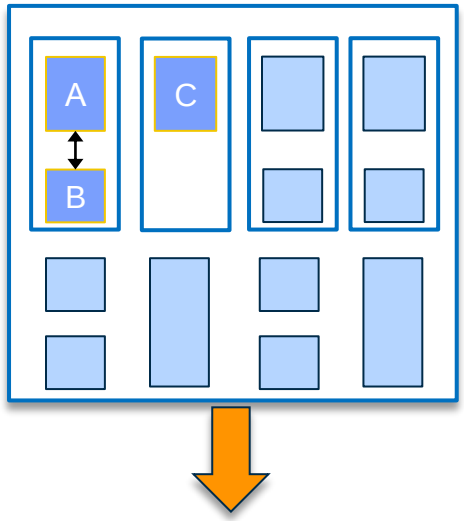
Get top design rtl/xml and connectivity reports

Hierarchy Manipulation

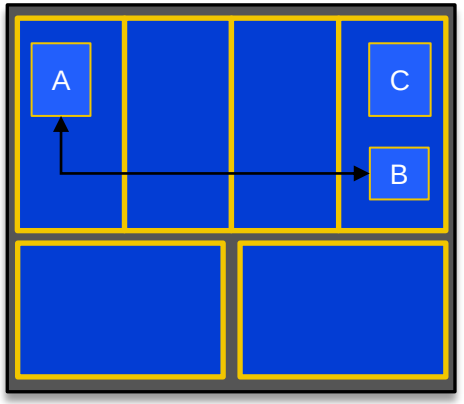
Fast and safe response to physical design requirements



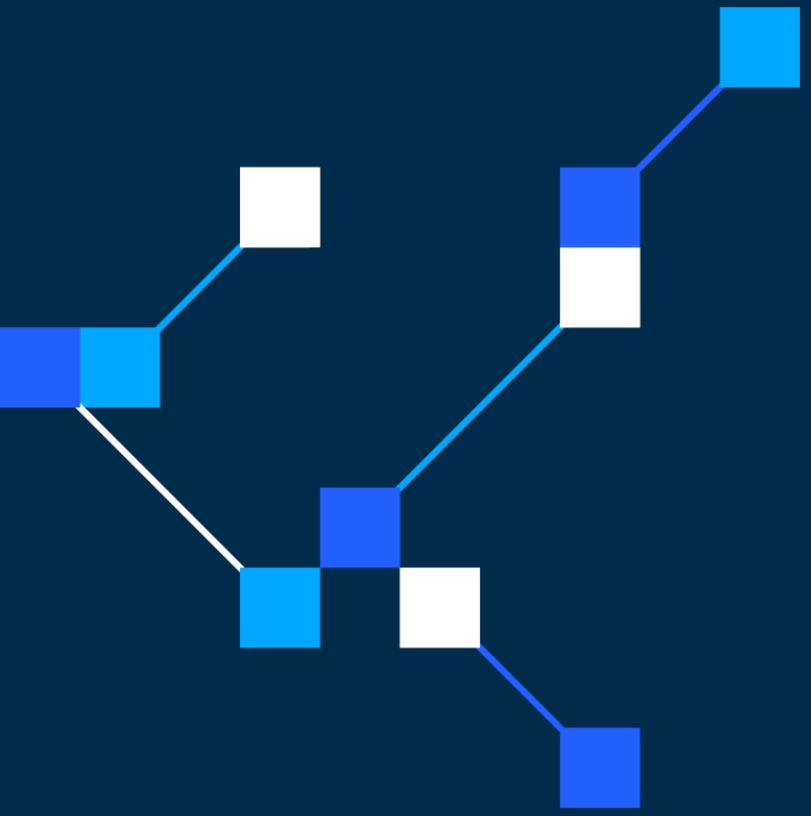
IP-XACT Design
from RTL Hierarchy



Physical Hierarchy
(Hard macros)

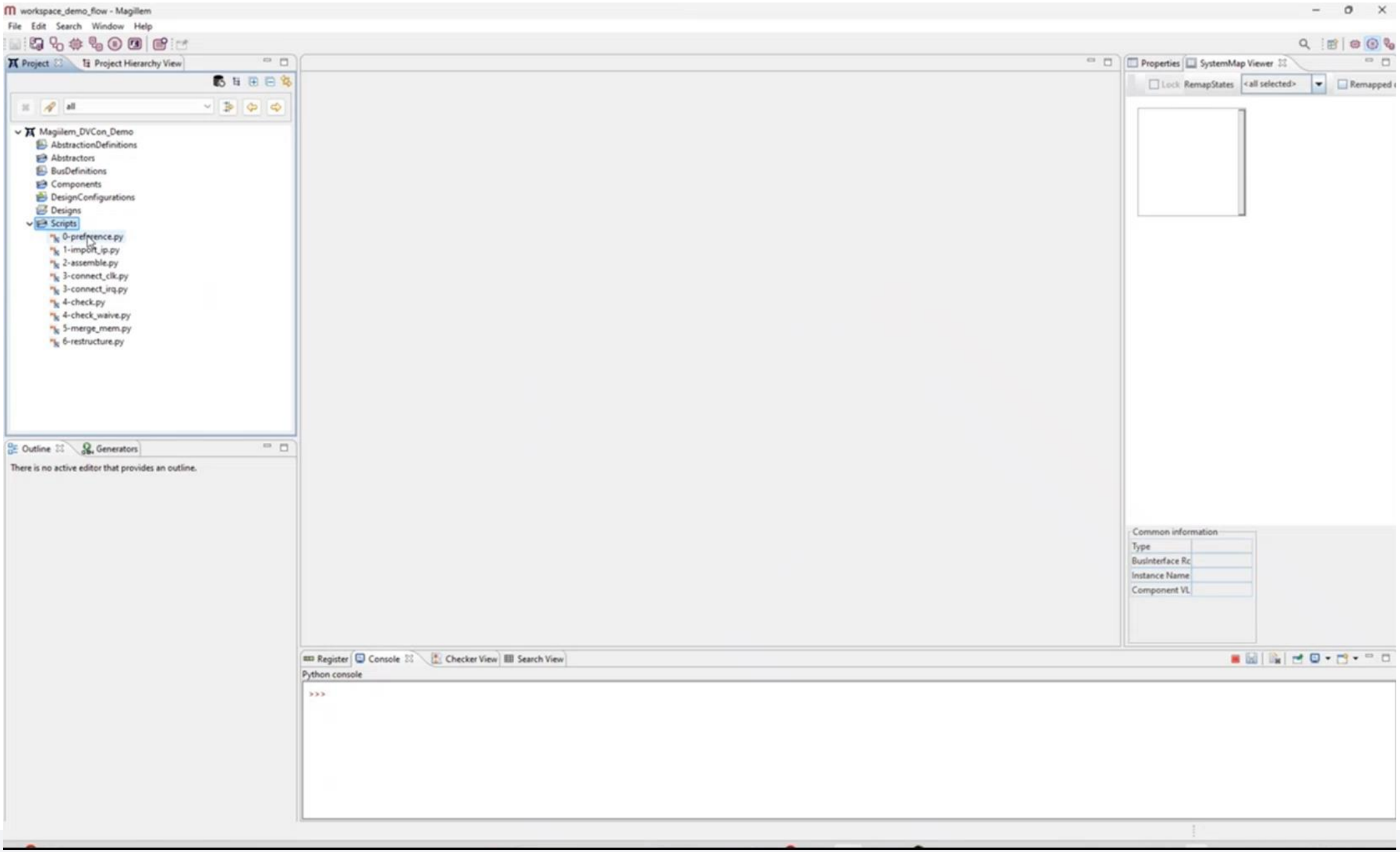


- Automated Move, Merge, or Flatten physical/virtual hierarchy:
  - RTL restructuring to meet power & floor-planning constraints
  - Partitioning (power, clock, and voltage domains)
  - Hard macro replication, Split SoC design in chiplets, Feedthrough connections for abutted floorplan
- Process reduced from weeks to 1-2 days



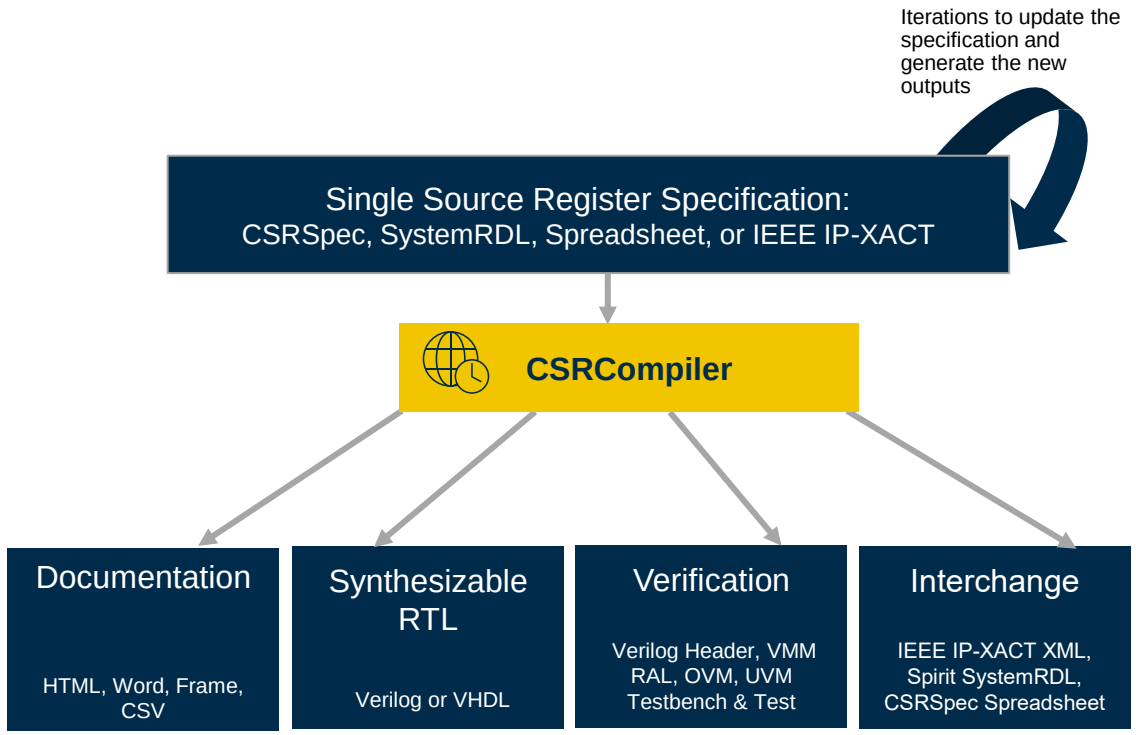
Demo

Magillem Integration Automation



ARTERIS IP

CSRCompiler
Automate Hardware/Software Interface (HSI)



Unified Specification and Compilation Flow

- Provide a scalable infrastructure that promotes a rapid, highly iterative design environment
  - up to 5 Million Registers
  - compile over thousands of registers in seconds, millions in minutes
- Built-in ability to validate IP from third-party or internal legacy
  - ensure data is clean, verified, and ready for use.
- True cross compiler
  - only one command in batch mode to read input and generate the needed output files
- Support of various formats for:
  - Import:
    - CSRSpec
    - IP-XACT
    - SystemRDL 2.0
    - More practical XLS import
  - Export:
    - IP-XACT, SystemRDL 2.0
    - FrameMaker, HTML, Docx
    - VHDL/SV/Verilog reg bank
    - UVM ral
    - C HAL

CSRCompiler Key Features

- Extensive error/syntax checking with over 1,000 error checks
- Highly configurable – over 6,000 combinations of register behaviors
- Time-saving templates support
- Industry-standard buses
- Registers broadcast/alias and virtual registers support
- Wide memories and atomic access support
- Back door path mapping
- Coverage bins
- Parity checks

For RTL Architects

Making your life easier: simple design capture and standardized, self-checking authoring; clean, standard RTL; 100% accurate.

For Software Developers

Benefits include: consistent documentation; single-source spec that generates both RTL and Header files; early software access.

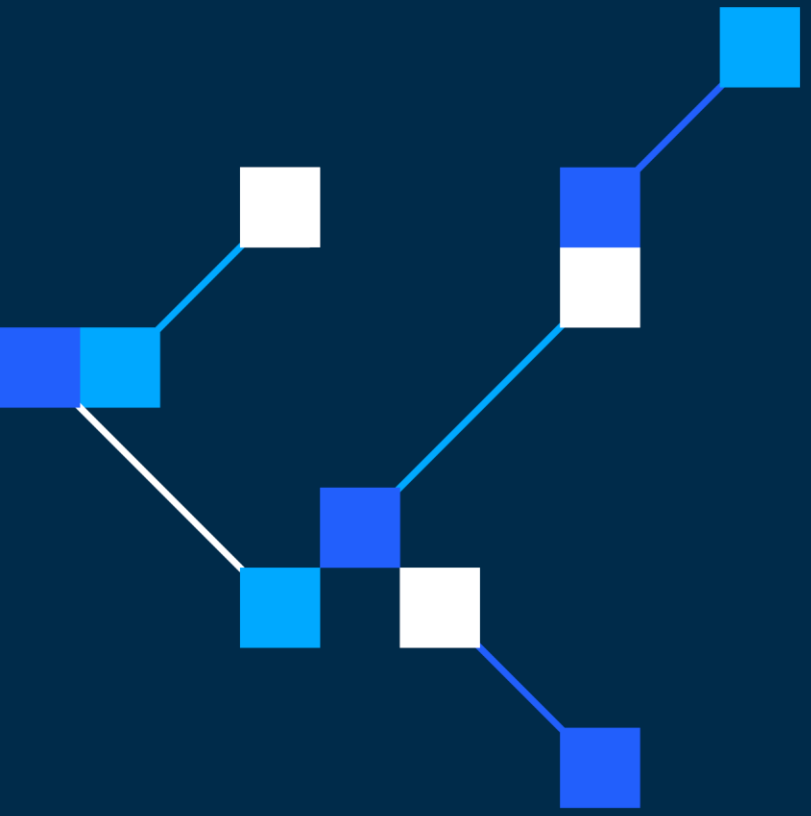
For Verification Engineers

Take advantage of: consistent documentation; a single-source spec that generates the SystemVerilog testbench register model and register information.

For Tech Pubs

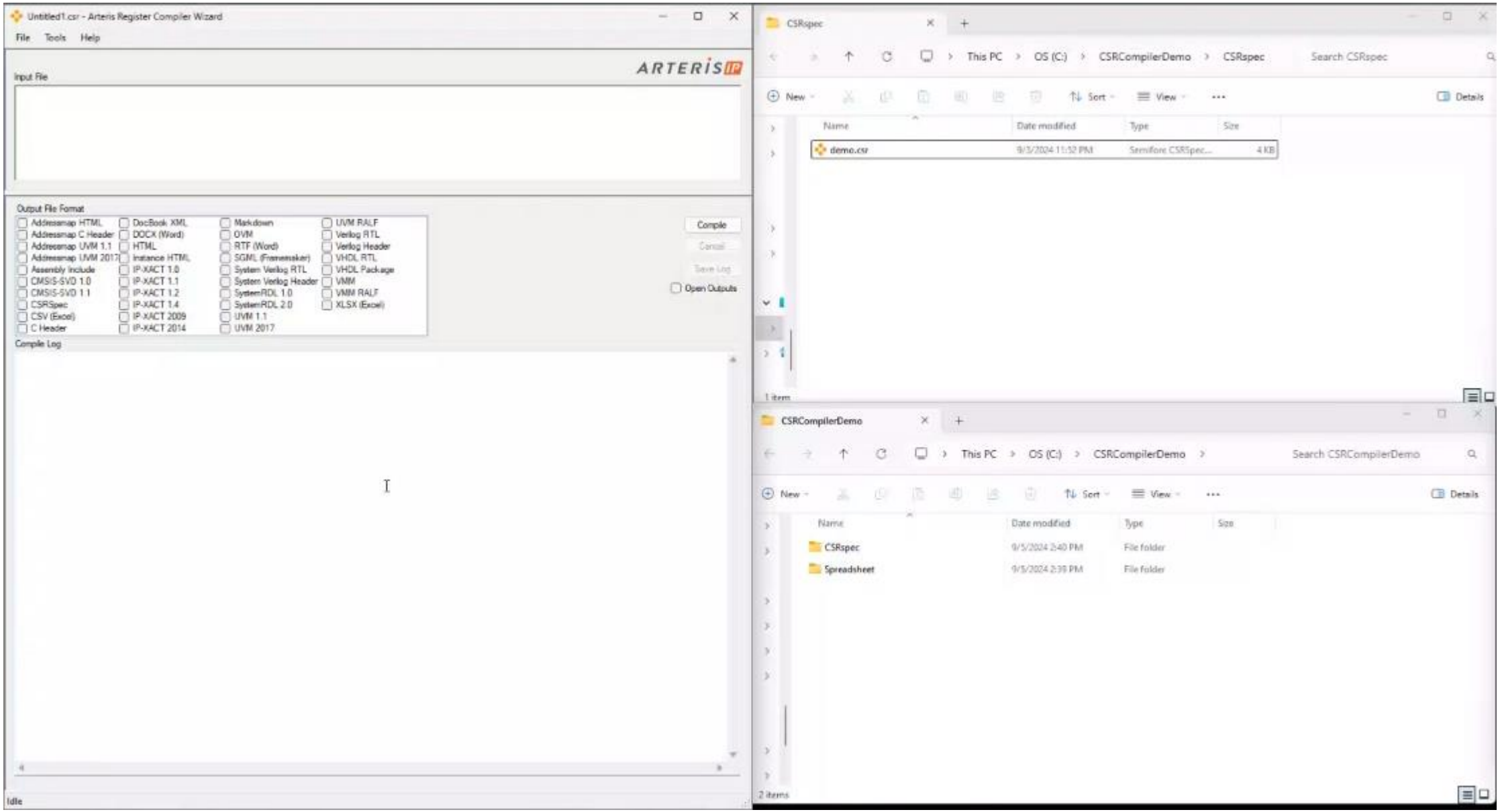
Always 100% accurate: 100% accurate documentation auto-generated in Word or FrameMaker; generate multiple document views and/or formats from the same source.

ARTERIS IP



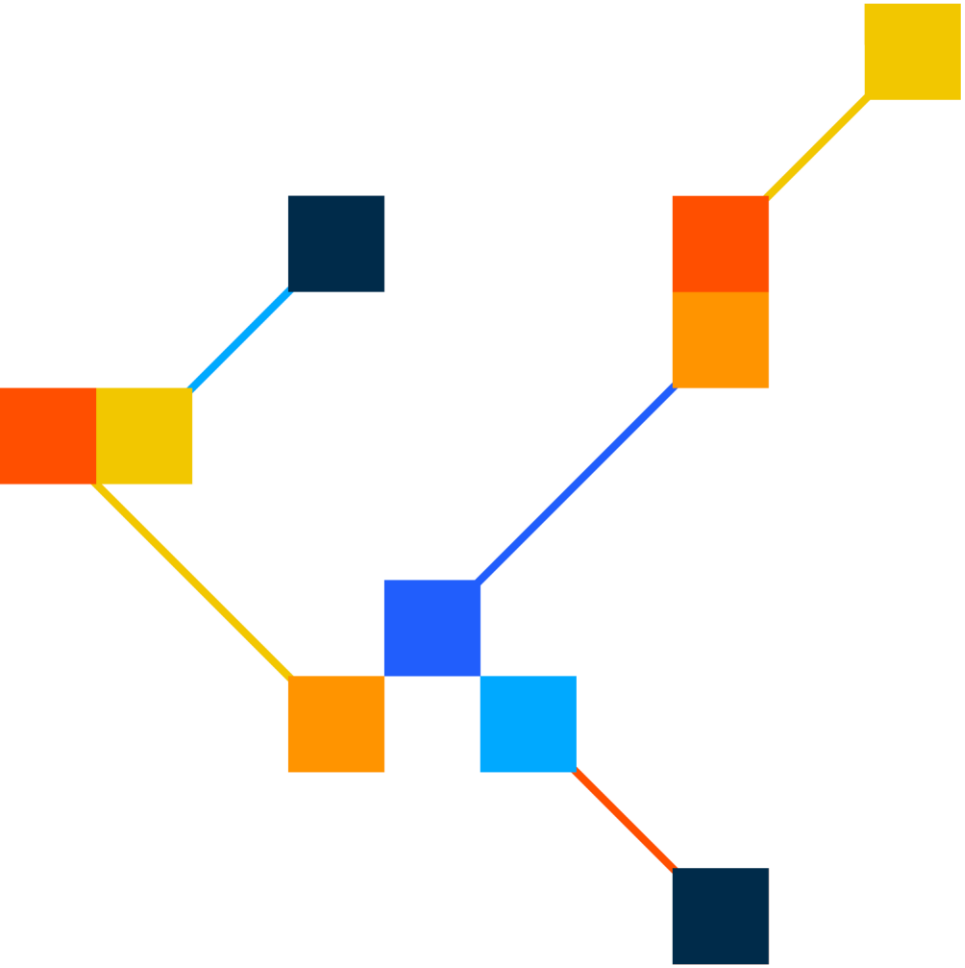
Demo

CSRCompiler Spreadsheet Flow



Arteris SoC Integration Benefits

- Shorten and streamline the IP integration process
  - For true IP Reuse methodology (IP and subsystems) with vendor-independent IP packaging (IP-XACT based)
  - Accelerate connectivity through automation
- Single Source of truth environment for system hardware/software design
  - Enable consistency and interoperability between the steps of a complex design flow
  - Ensure system memory map validation
- Correct by construction design: Capture → Check → Generate
  - Catch errors as you enter the design information before running any simulation
  - Higher quality designs
- Continuous Integration with a robust SoC build process
  - Quickly and safely react to design changes (update central data model) to meet changing needs
  - Our solution is scalable and repeatable on design derivatives, projects, and design flows
- Improve design productivity with a first-time-right process
  - Empower design teams to hit time to market, achieving successful tape-outs on time.
  - Leverage technical expertise and focus on core business



ARTERIS IP

Thank you