Dynamic Switching Performance of GaN HEMTs in Boost Converter Topology Using Double Pulse Test (DPT) with Parasitic-Induced Effects

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Agenda

Abstract

Introduction & Motivation

**Circuit Structure**

Result & Discussions

Conclusion

Abstract

This work presents a detailed evaluation of GaN HEMTs switching performance in a Boost converter using the Double Pulse Test (DPT) under practical conditions. The test setup involves a drain-source voltage (V_{DS}) of 50V and a gate-source voltage (V_{GS}) swing from –3.8V to 6.2V. Results highlight the significant influence of parasitic inductances at the gate, drain, and source terminals on switching behavior. Simulations in LTspice reveal effects such as voltage overshoot, current ringing, and elevated switching losses. The study importance of minimizing parasitic elements through careful PCB layout and packaging to enhance efficiency, reliability, and performance in high-speed GaN power converters.

Introduction & Motivation

- ## Why Study GaN HEMTs in Boost Converters?

  - GaN HEMTs offer faster switching and lower losses compared to Si/SiC MOSFETs
  - **Boost converters are widely used** in EVs, solar inverters, power supplies, and industrial applications.
  - **GaN HEMTs switching behavior in Boost topology** helps designers optimize power density, thermal performance, and system reliability.
  - Using DPT to analyze real-world switching behavior, including the impact of parasitic elements.
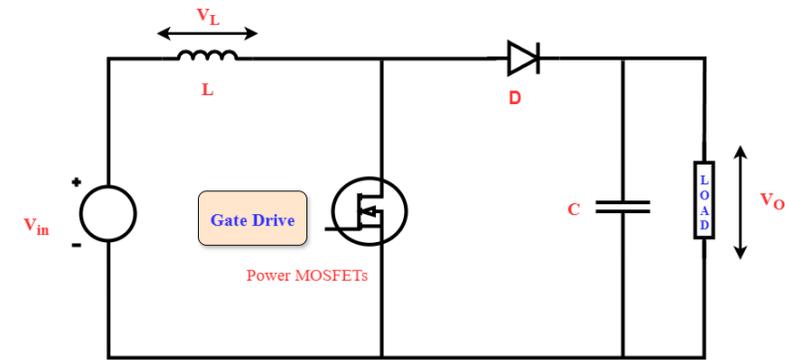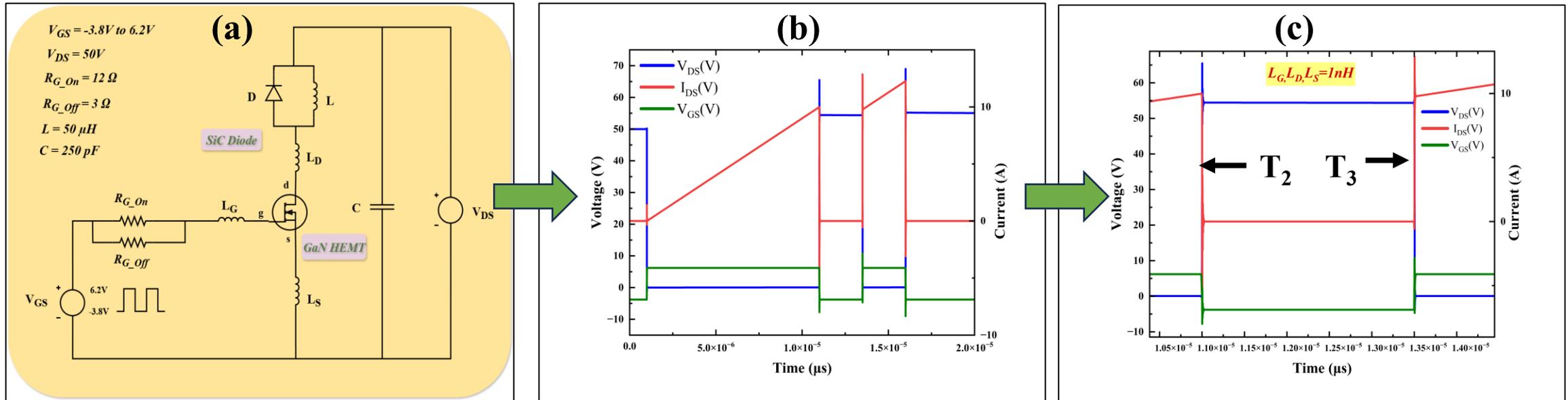

Boost Converter

Boost Converter using DPT

V_{GS} = -3.8 V to 6.2 V
V_{DS} = 50V
I_{DS} = 10A
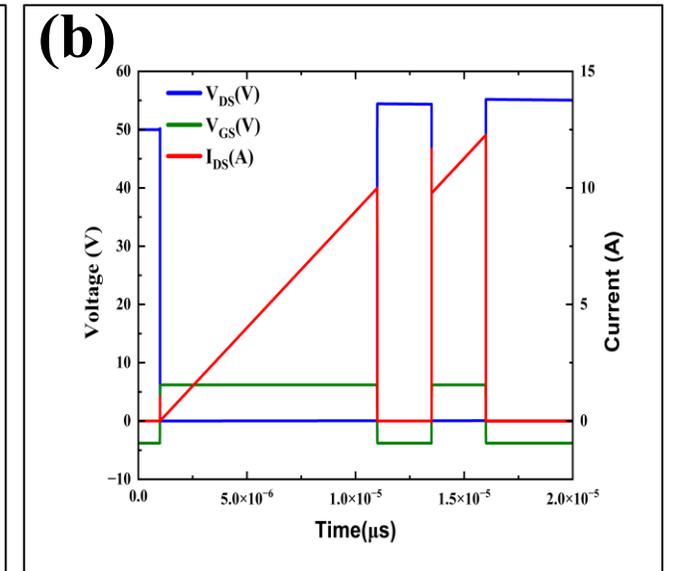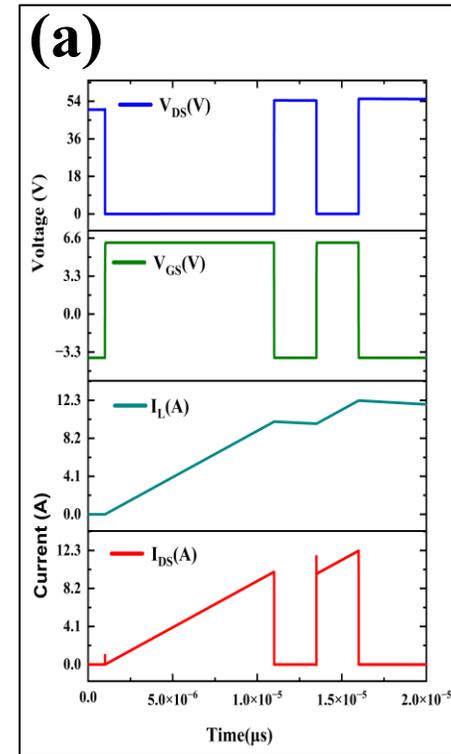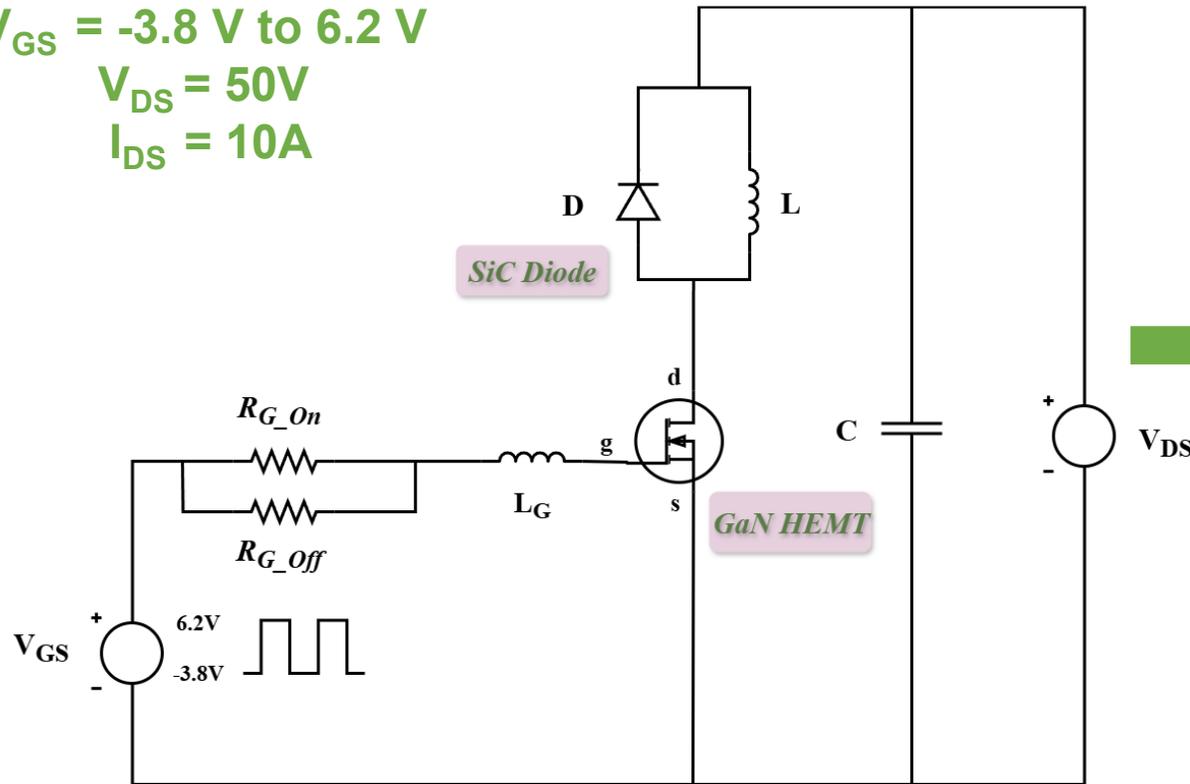
Schematic of a Boost Converter Using GaN HEMTs Under Double Pulse Test (DPT)

**Output Voltage and current waveform of Boost Converter using DPT**

Parasitic-Induced Effects in DPT(L_G, L_D, L_S=1nH)

(a)

V_{GS} = -3.8V to 6.2V
V_{DS} = 50V
R_{G_On} = 12 Ω
R_{G_Off} = 3 Ω
L = 50 µH
C = 250 pF

(b)

(c)

L_G, L_D, L_S=1nH

T_2 T_3

## Parasitic-Induced Boost Converter in DPT

- Gate and power loop parasitics cause voltage overshoot and current ringing.
- Parasitics increase switching losses and electromagnetic interference (EMI).
- Parasitic effects directly impact switching waveforms and device reliability.

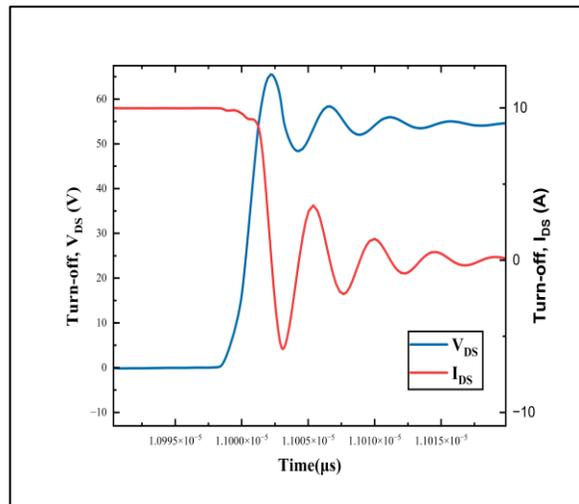# Switching Characteristics(With & without Parasitic inductor)
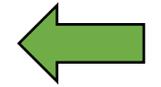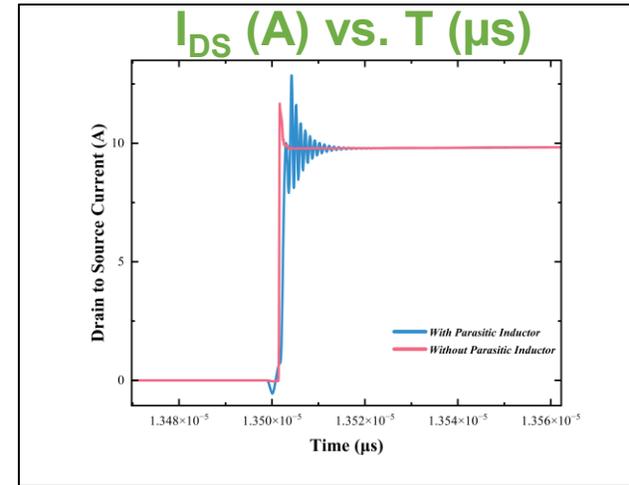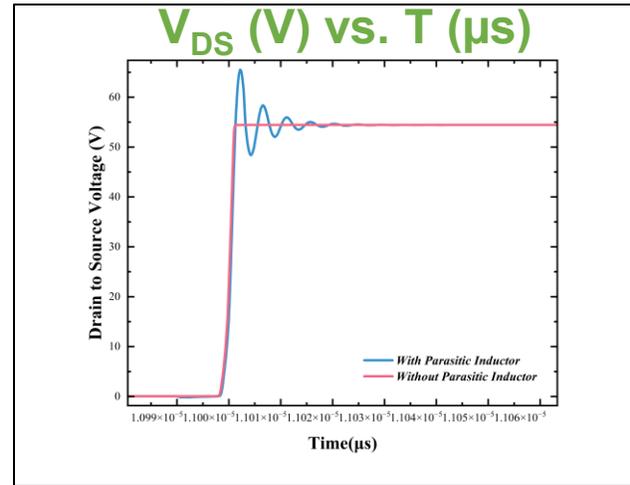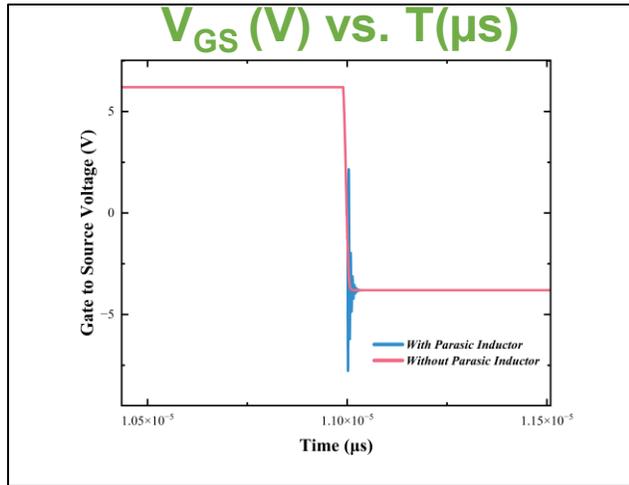
Turn - ON Switching Transient
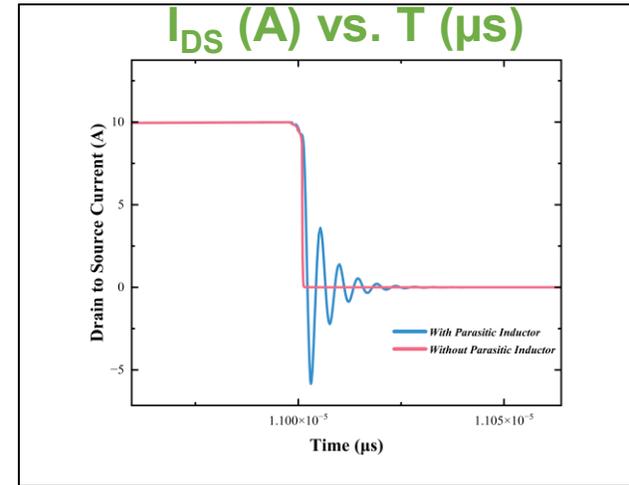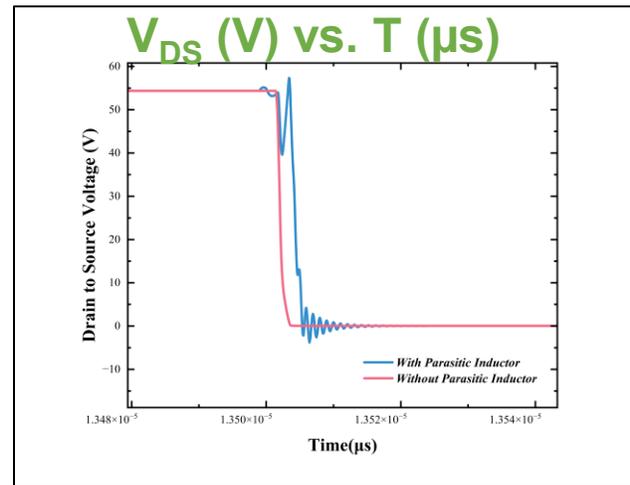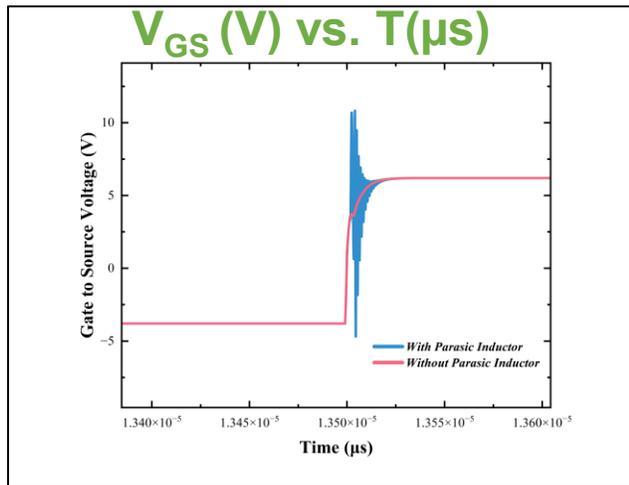
Turn - OFF Switching Transient

Switching Loss Analysis in DPT Test
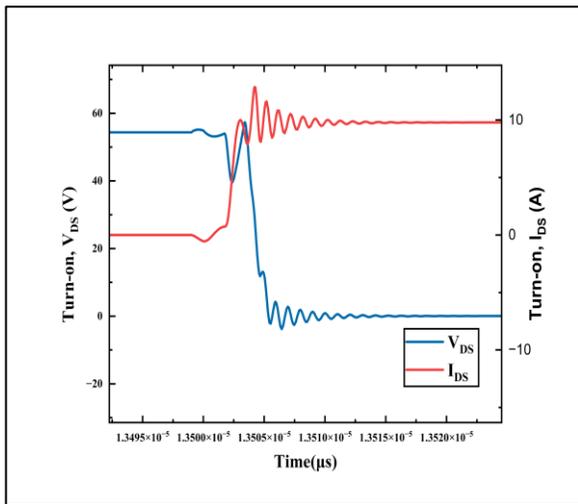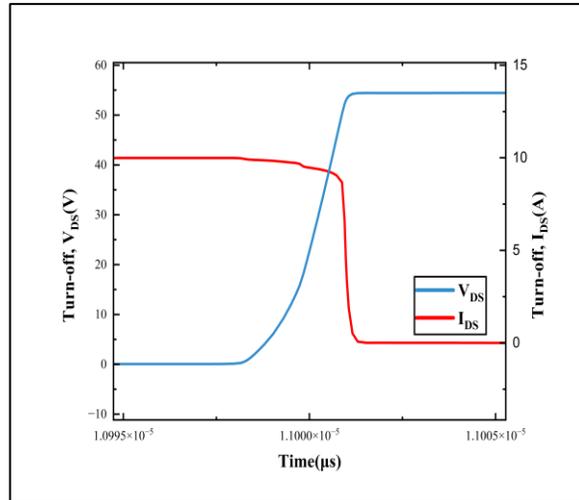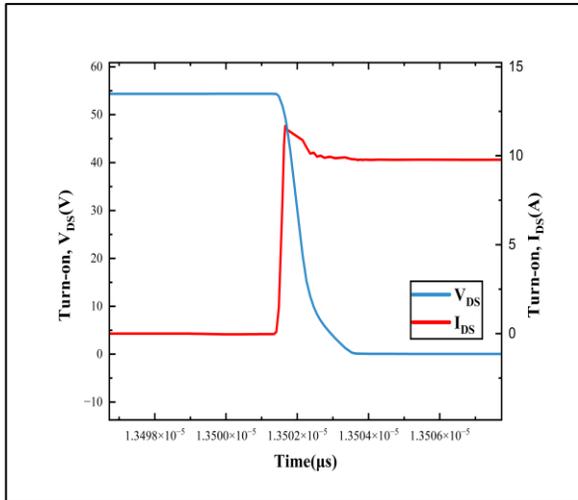
Turn - ON
Switching loss in DPT

Parameter	Switching energy and power loss for different GaN HEMTs configurations under f_{sw}=66.52kHz			
	E_{on}	E_{off}	E_{total}	P_{sw} (mW)
Fresh (without Parasitic Inductor)	335.85nJ	473.78nJ	809.63nJ	53.8mW
With Parasitic Inductor (L_G,L_D,L_S=1nH)	972.38nJ	779.76nJ	1.752µJ	116.6mW

Turn - OFF
Switching loss in DPT

Conclusion

- Double Pulse Testing (DPT) is an effective method for evaluating dynamic behavior and quantifying switching losses.

- GaN HEMTs offer superior switching performance over Si/SiC MOSFETs, enabling high-efficiency boost converter operation.

- Parasitic elements significantly impact switching waveforms, causing **Voltage overshoot, ringing, and increased switching losses**.

- Proper layout design and parasitic minimization are essential GaN devices power conversion.

- Future work will focus on optimizing **power loop design and integrating advanced gate driver techniques** to further reduce losses.

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Q&A

Thank you for your attention and participation!
I welcome your questions and feedback.

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