2025 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION TAIWAN

EP-Ready Hardware-Assisted-Verification Platforms

Common Hardware, Multiple Use-Cases

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SYNOPSYS®

accellera SYSTEMS INITIATIVE

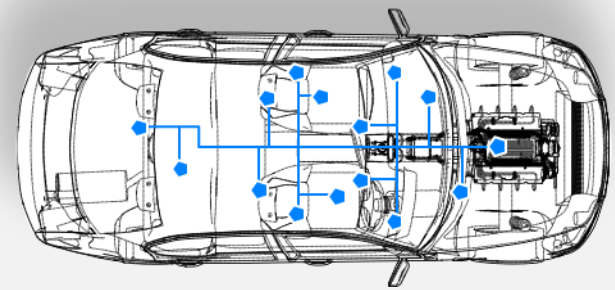
Agenda

- Industry Trends & Challenges
- What Is EP-Ready?
- How can EP-Ready Platform Helps?

Industry Trends & Challenges

Pervasive Intelligence

Autonomy and software-defined systems reshaping industries

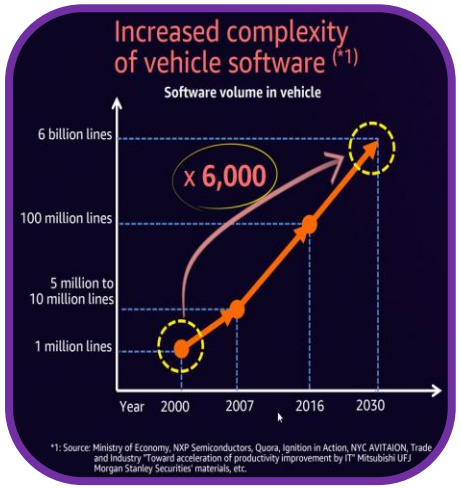


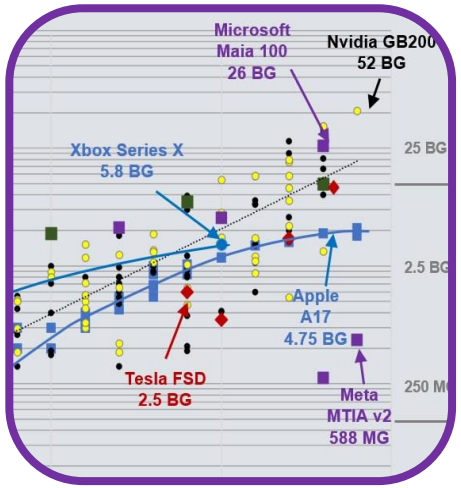
Systems companies re-architecting products, business models and development processes

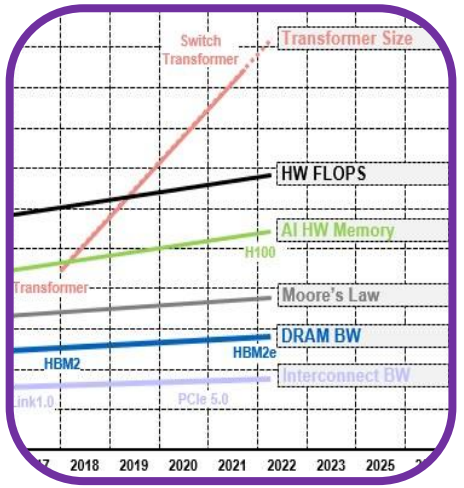
Driving demand for massive compute, both at the edge and the data center

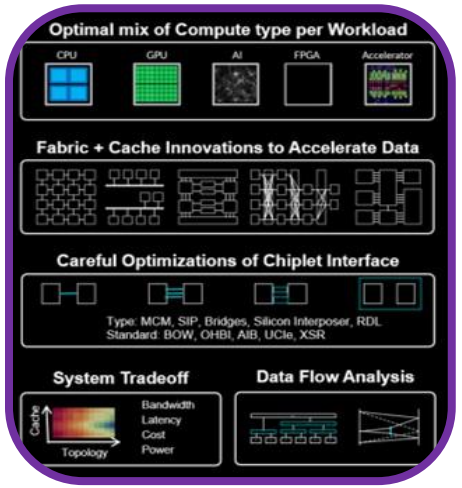
Verification Challenge: Quadrillions of Cycles

Software **Hardware** **Interfaces** **Architectures**









The keystone for ensuring functionality, power and performance

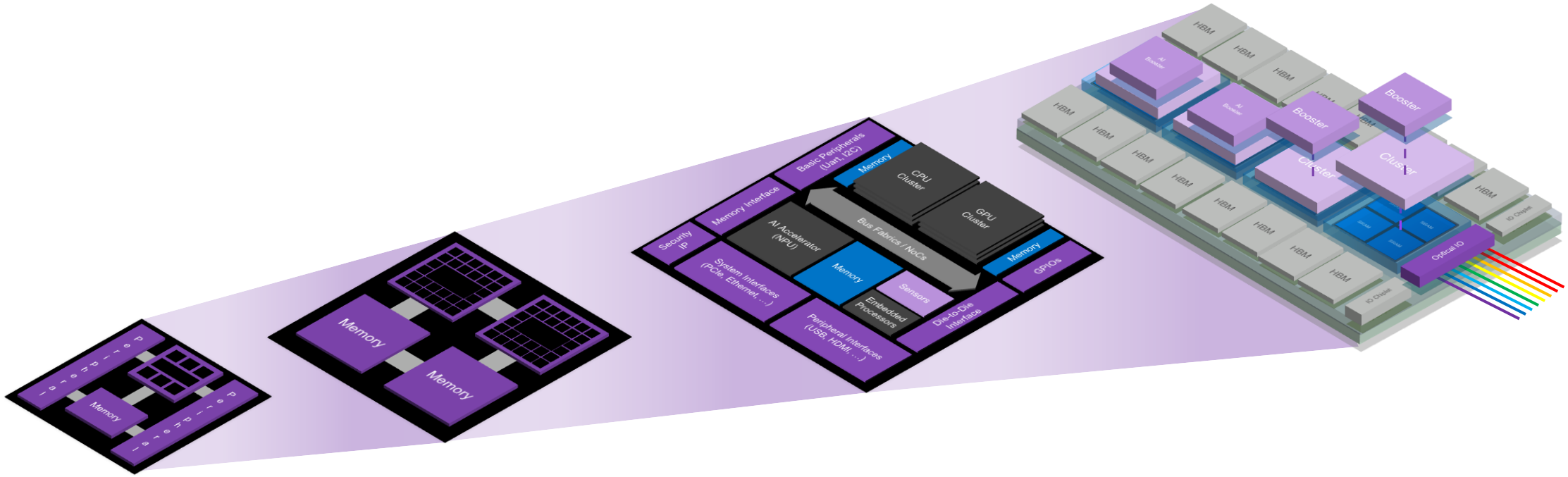
Sources: AWS, Synopsys, AI and Memory Wall: 2403.14123 (arxiv.org), Baya Systems, *"What Makes RISC-V Verification Unique?" https://bit.ly/4hDXCe9

Verification Happens in Phases!

Simulation 10s Hz

Silicon At Speed

Hardware Assisted Verification (HAV)

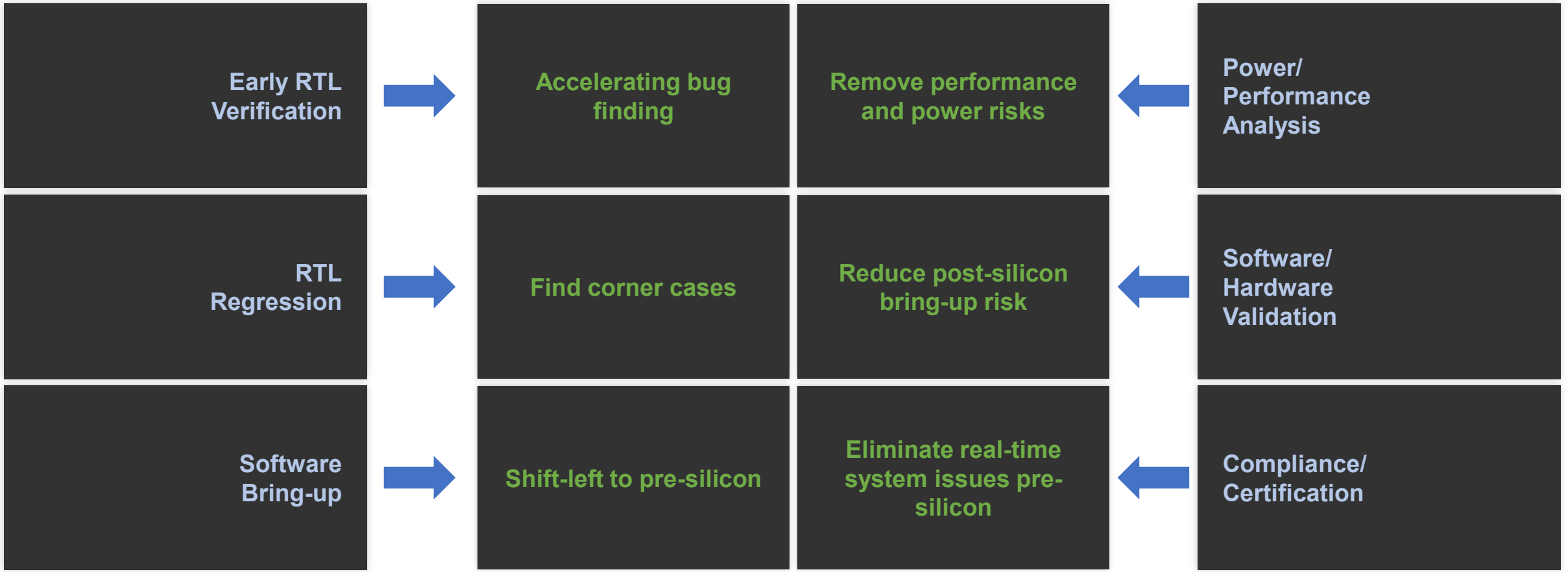


IP/Core Centric → Subsystem / Software → Full Chip(let) / Software → Multi-die / Software

*"System Validation at ARM: Enabling our Partners to Build Better Systems", https://bit.ly/3WLCvhr, https://bit.ly/3CEMBd0

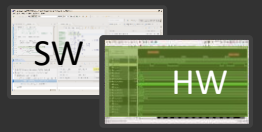
What is EP-Ready?

Many Use Cases drive Verification Cycles



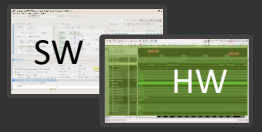
Use Cases Require HAV Engine Trade-offs

Hardware-Assisted Verification Solutions



Verdi & VCS

Early RTL Verification



Verdi & VCS

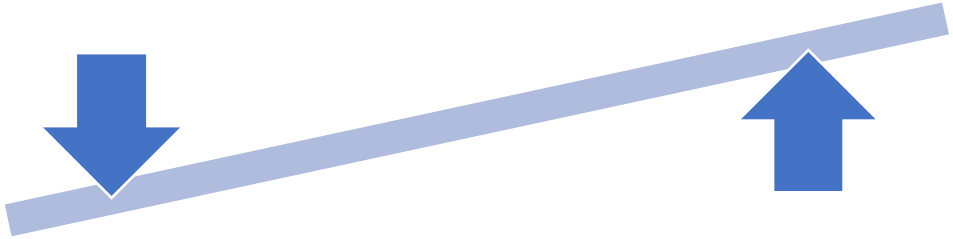
RTL Regression

Virtualizer

Software Bring-up

Emulation (ZeBu Software)

- Single step, full visibility debug for RTL verification
- Full cycle accuracy for performance validation
- Cycle by cycle activity for accurate power estimation



Prototyping (HAPS ProtoCompiler)

- Ability to optimize IP and subsystem performance
- Highest performance for SW bring-up on RTL models
- Protocol compliance and certification testing at speed

Power/ Performance Analysis

ZeBu Empower

Platform Architect

Software/ Hardware Validation

HAPS Protocol Interface Card

Speed Adaptor

Compliance/ Certification

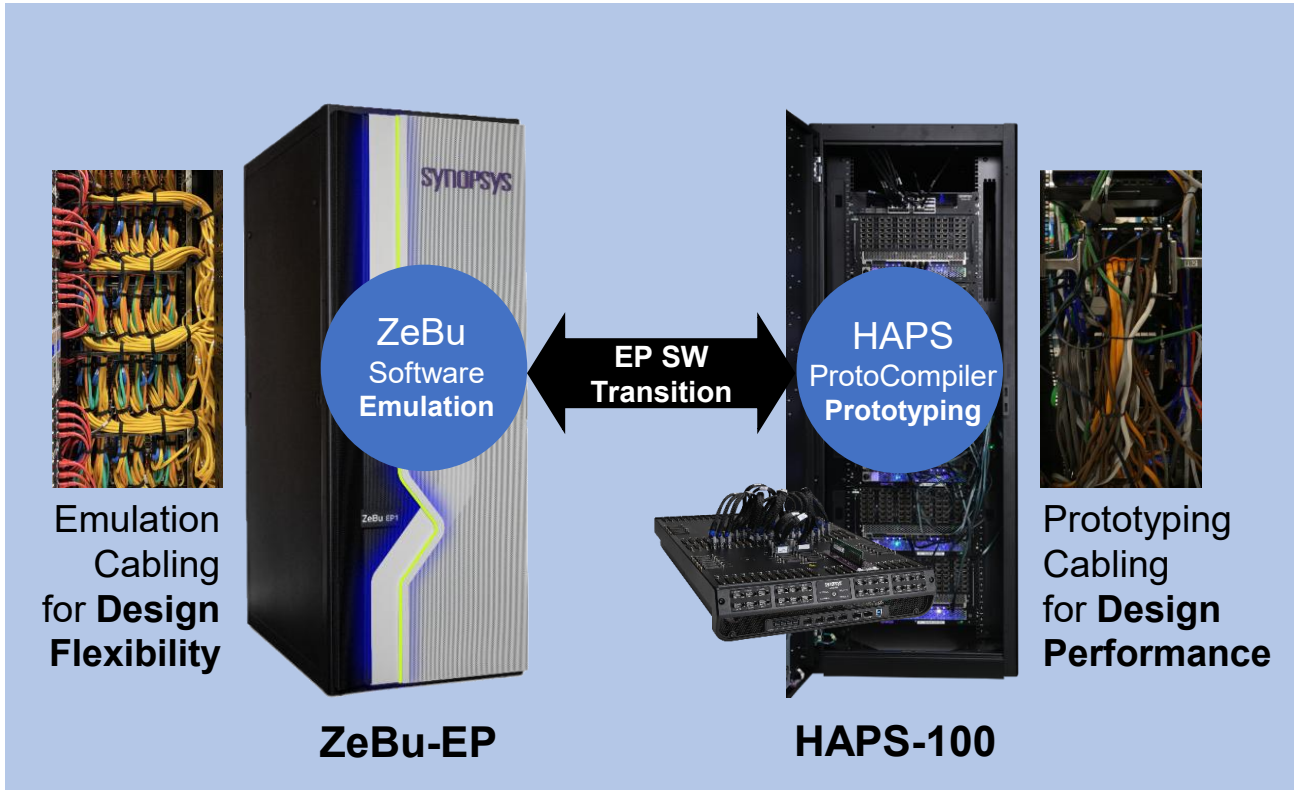
HAPS IP Prototyping Kit

Synopsys EP-Ready Hardware

Extended Synopsys **Emulation and Prototyping Ready (EP-Ready) Hardware**

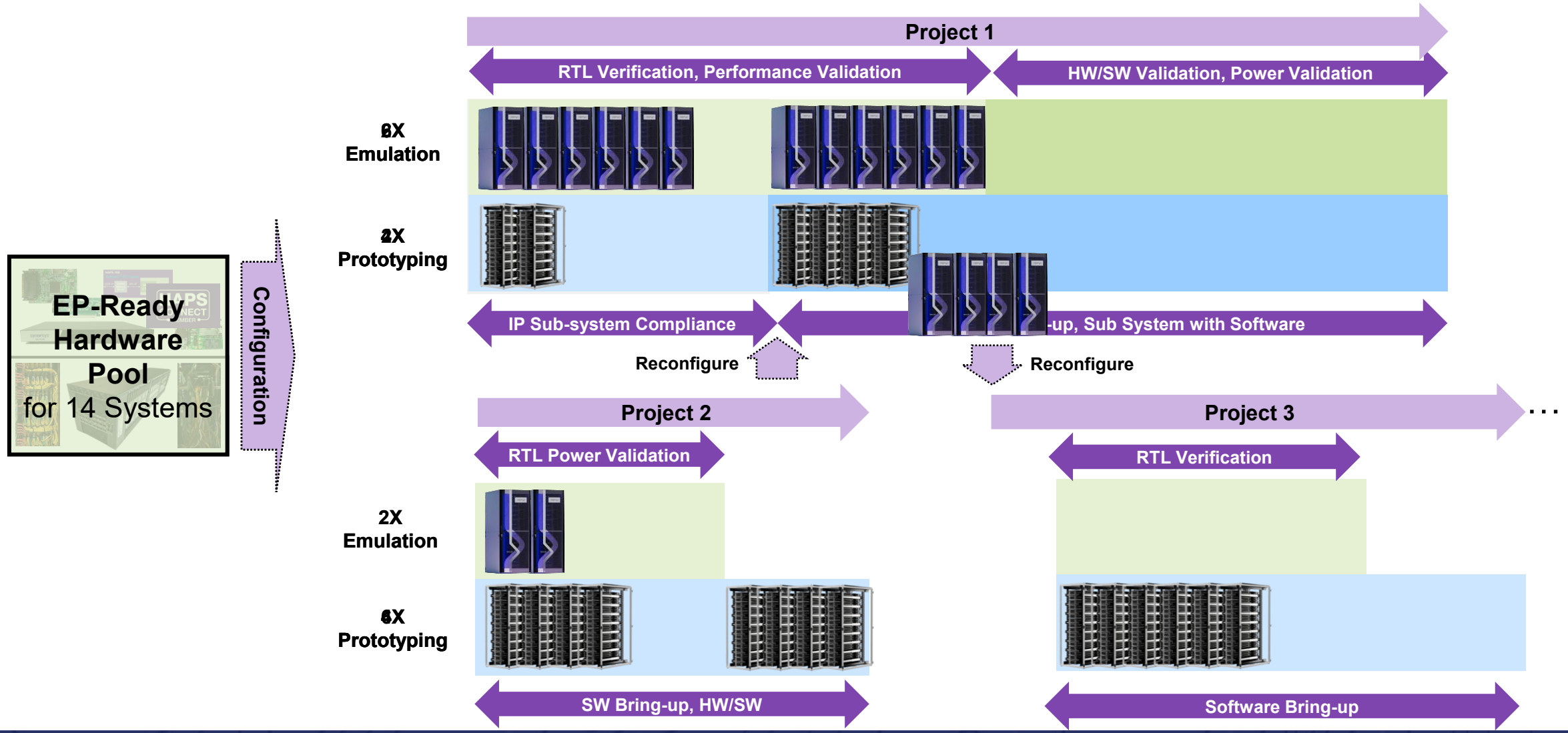
- **one** hardware platform
- **configurable** for emulation or prototyping
- **two** software stacks

- **all** emulation and prototyping **use cases**
- optimize **ROI** to get the **most for your budget**
- **eliminate** the **need to decide balance** of emulation and prototyping hardware up front



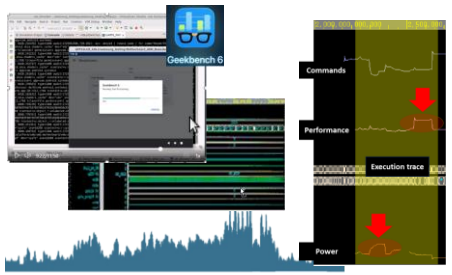
How can EP-Ready Platform Helps?

Best ROI for Emulation & Prototyping Use Cases



Configurability for EP-Ready Hardware

Emulation Use Cases



Prototyping Use Cases

ZeBu Software

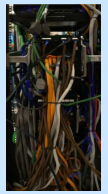
User Design

HAPS ProtoCompiler

Interfaces Memories

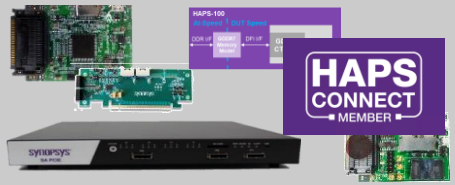
Interfaces Memories

Cabling for **Design Flexibility**



Cabling for **Design Performance**

Configurability for EP-Ready Hardware

			Emulation	Prototyping
Use Cases		Early RTL Verification	☑	
		RTL Regressions	☑	☑
		Software Bring-up	☑	☑
		Software/Hardware Validation	☑	☑
		Power/Performance Analysis	☑	
		Compliance/Certification		☑
Software Stack		Compile	ZeBu SW	HAPS Protocompiler
		Debug	Comprehensive, Full Visibility	High Visibility, Fast
		Runtime	Flexible, Relocation	Design Dependent
		Clocking	Synchronous	Asynchronous
Interface Protocol Solutions		Memory Models	☑	Selected availability
		Transactor Models	☑	
		Speed Adaptors	☑	☑
		IP Prototyping Kits		☑
Hardware Platform		Scalable Connect – Hubs	☑	
		Cabling Setup	Optimized for Design Flexibility	Design Dependent
		Direct Connect – Cables	☑	☑
		Base Module		

Synopsys HAV Product Family

Highest Scalability, **Best Density**

NEW

HAPS-200 & ZeBu-200

Highest Performance, **EP-Ready Hardware**

Thank You