2025 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION TAIWAN

Modernizing Hardware/Software Interface
Bringing your register design into 21st Century

YiChiang Chang
YiChiang.Chang@arteris.com

ARTERIS IP

accellera SYSTEMS INITIATIVE

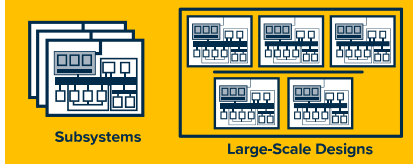
Arteris SoC Integration Automation

Magillem Connectivity

Protocols | RTL | IP

Import and IP Packaging
Port, parameter, bus interface, source files(fileset)

SoC Assembly
(Instantiate, Configure, Connect, Hierarchy, Restructuring, Partition, Incremental design)



IP IP

API libraries
(TGI, RTL, etc.)

Elaborated Data Model
IP-XACT

CLI
(Python, Tcl)

Flow Automation

Checkers (Std + Customs) + Reports

Generators (Std + Customs)

UPF | AMD XILINX | SYNOPSYS | cadence | SIEMENS


HDL top level netlist

Magillem Registers

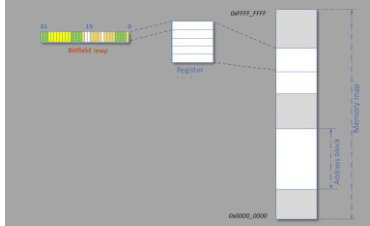
IP-XACT | CSRSpec | SystemRDL

Import
Memory map, bridge definition

IP

IP Packaging

HW/SW Interface
(Capture, editing, visualization, registers, bitfields,
System Map calculation)



Checkers + Reports

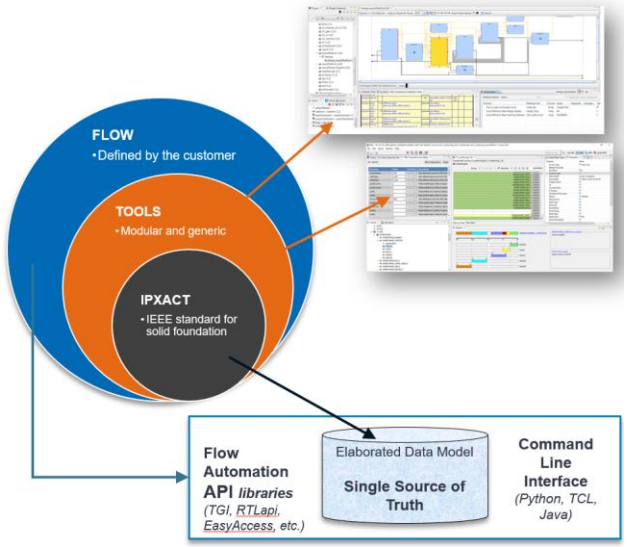
Generators (Std + Customs)

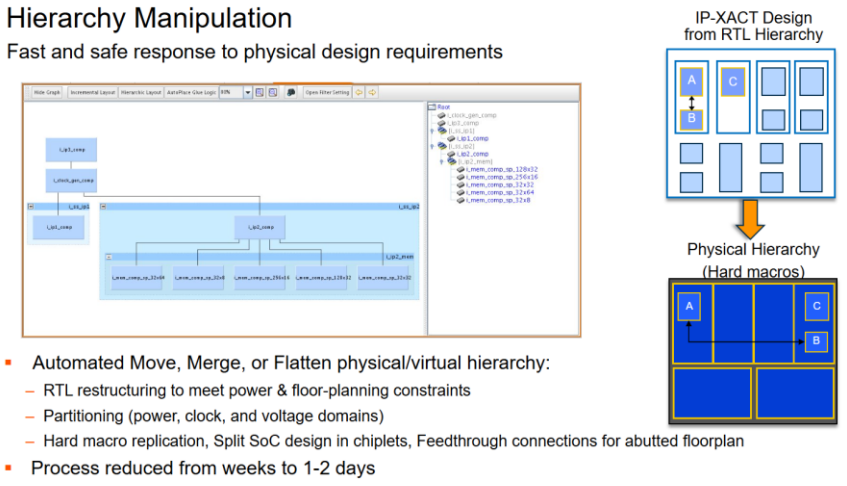
W | html | RTL | UVM | C hal

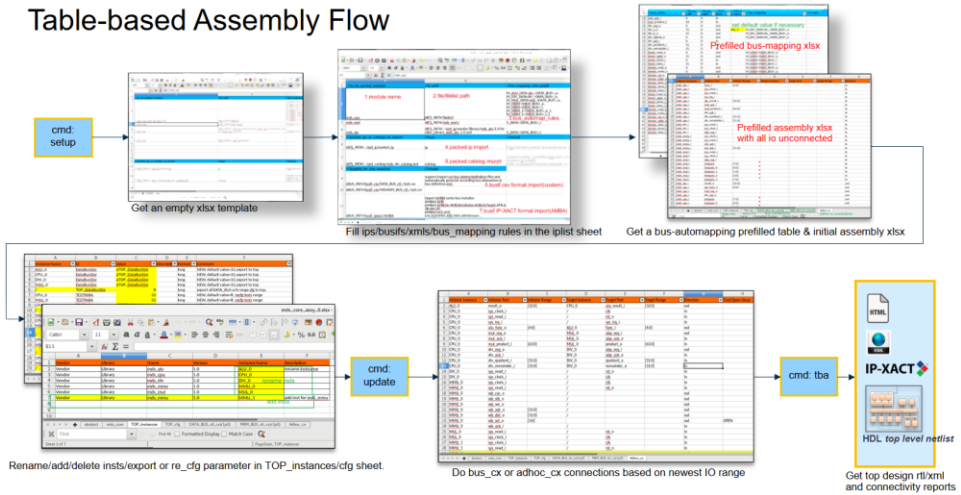
- Easy Configuration
- Continuous Integration
- Automated Generation
- Faster Cycle Time to Completion
- Better Quality
- IP Reuse
- Generate Derivative Designs

Magillem Connectivity

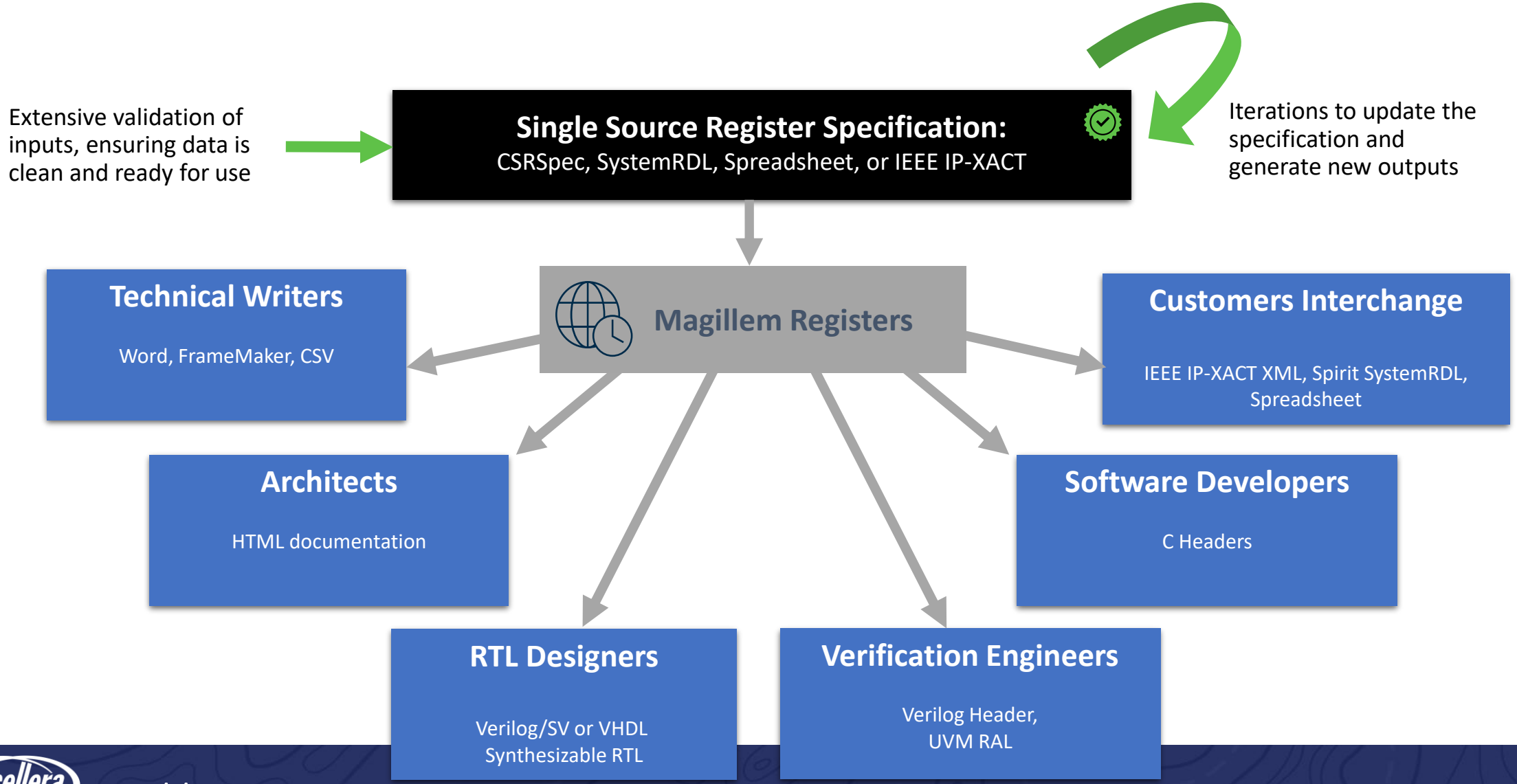
- **Features**
  - Project management and central database
  - IP and design reuse (IP-XACT packaging)
  - SOC design build, assembly, derivatives and outputs
  - APIs, custom features by APIs
  - Checkers and reports
  - Excel table flow
  - RTL restructuring
  - Hierarchy manipulation
  - GUI or batch mode



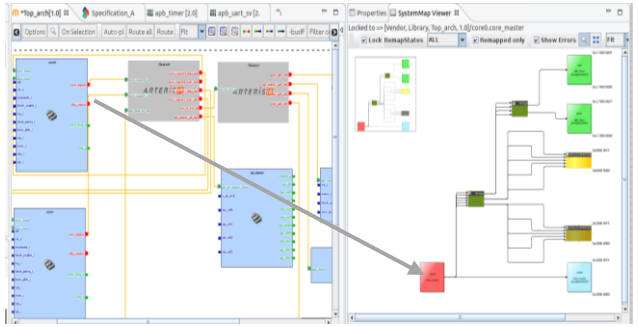




Magillem Register Automate HSI



Magillem System Map Flow



3rd party IPs

Component
IP-XACT 2022

Legacy IP

Component
MRV parameters
IP-XACT 2009

xml Convert 2009 -> 2022

Component
MRV VE
IP-XACT 2022

Write IPXACT2022

Component
MRV VE
IP-XACT 2022

SoC Architecture Specification

CSRSpec

Project Resources

System Map Import

Connectivity

Design

IP-XACT

SystemMap

Magillem Register

Fm HTML W UVM C/C++ & Assembly Headers

CSRSpec
SystemRDL
IP-XACT
Spreadsheet

Magillem Register

Component
Fileset: CSRSpec
IP-XACT 2022

Fm HTML W UVM Verilog/VHDL Synthesizable RTL Implementation

- Segments support
- System Map elaboration
- Registers are packaged in IP-XACT component

Magillem Register IDE for Script Development

- Unified environment to create/debug/execute scripts (Python and TCL)
- GUI based on Visual Studio Code
  - Flexibility, extensibility, and support for various programming languages and tools
  - Provide syntax highlighting, code completion, and linting
  - Native support for editing and validating XML-based files
  - Built-in support for Git integration allowing collaborative work on EDA projects
  - Easy to add your own plug-ins

❖ Note: Magillem is also available in pure shell (interactive or batch) mode

Technical Capabilities

1. Highly scalable: Up to 5 Million Registers
2. True cross compiler: All specification formats supported for input and output
3. High-quality RTL: Extensive error checking
4. Powerful generator: RTL reg bank, UVM, C-HAL, Documentation…
5. Highly configurable: Over 400 configuration properties
6. Advanced features support: Wide memories, alternative UVM backdoor methodology for high performance on large designs

Thank you